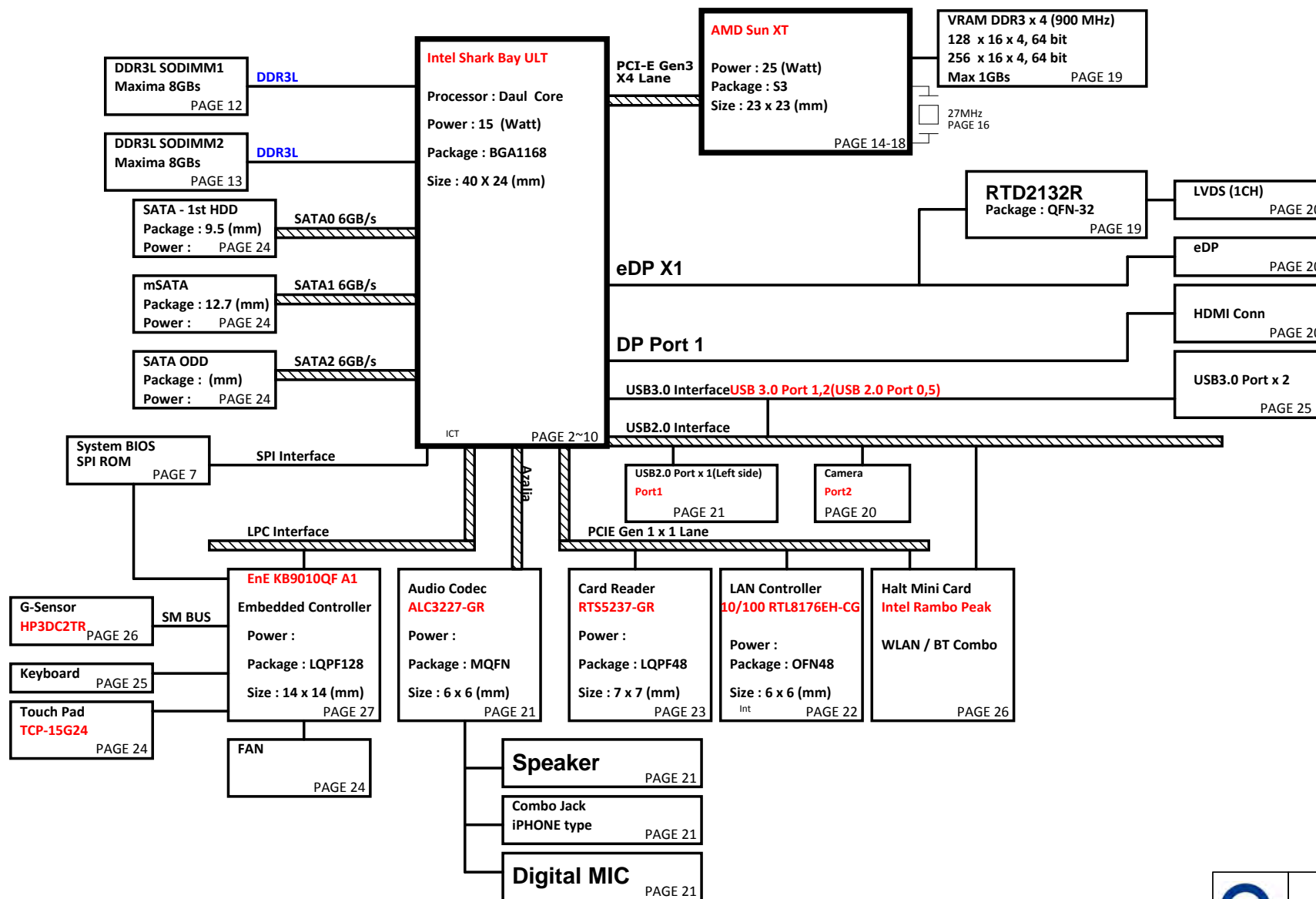


U83 DIS (14"/15.6") Ultra/Slim Intel Shark Bay ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT





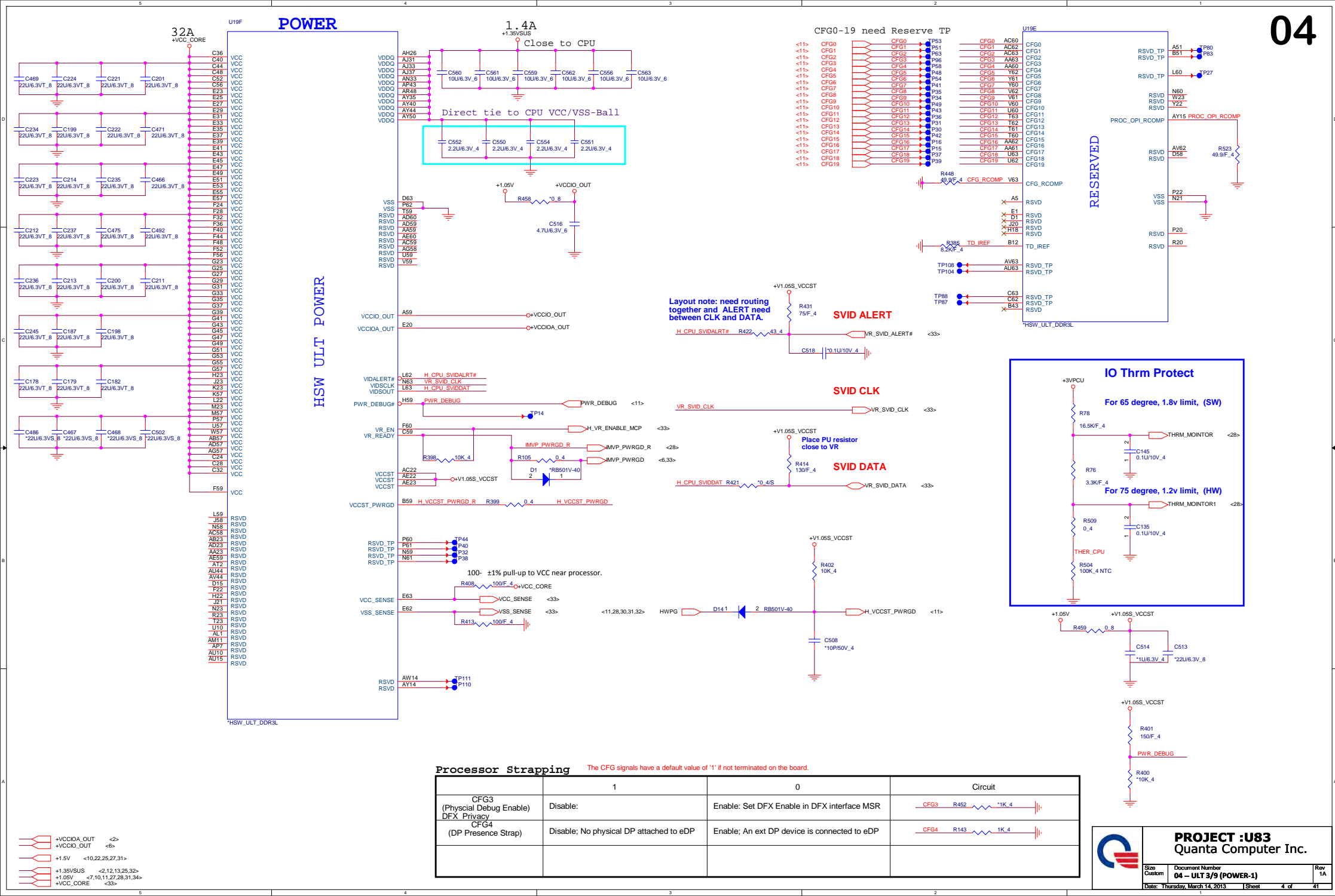
Processor pull-up (CPU)

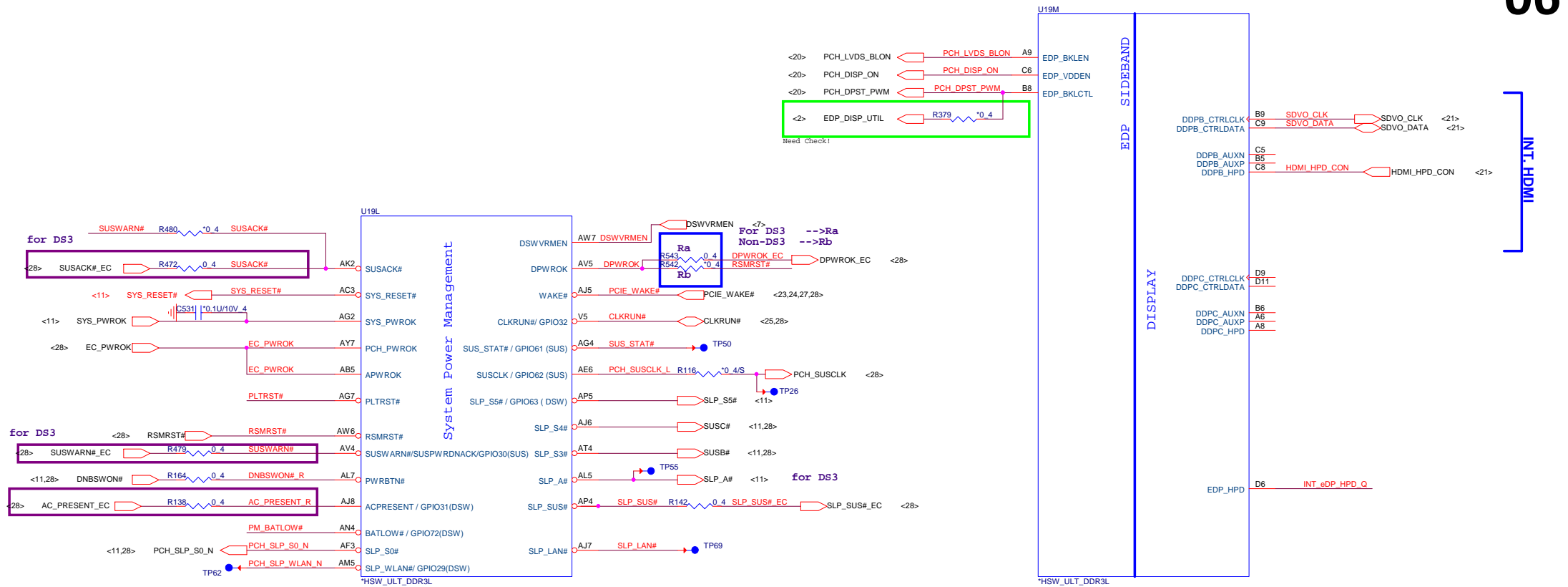


The diagram illustrates the memory controller architecture for the U83, showing the connection between the U19C and U19D chips and the DDR SYSTEM MEMORY A and B banks. The U19C chip is connected to the DDR SYSTEM MEMORY A bank, while the U19D chip is connected to the DDR SYSTEM MEMORY B bank. The diagram includes signal traces for address, data, and control signals, with labels for various memory banks and signal names.

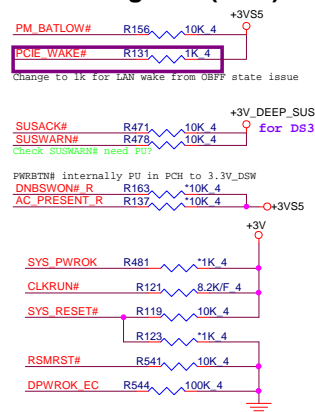
U19C Connections:

- SA_CLK0:** Connected to U19C pin AV37.
- SA_CLK#0:** Connected to U19C pin AU37.
- SA_CKE0:** Connected to U19C pin AU43.
- SA_CLK1:** Connected to U19C pin AY36.
- SA_CLK#1:** Connected to U19C pin AW36.
- SA_CKE1:** Connected to U19C pin AW43.
- SA_CKE2:** Connected to U19C pin AY42.
- SA_CKE3:** Connected to U19C pin AY43.
- SA_CS#0:** Connected to U19C pin AP33.
- SA_CS#1:** Connected to U19C pin AR32.
- SA_ODT0:** Connected to U19C pin AP32.
- SA_DQS#0:** Connected to U19C pin AJ61.
- SA_DQS#1:** Connected to U19C pin AN62.
- SA_DQS#2:** Connected to U19C pin AM68.
- SA_DQS#3:** Connected to U19C pin AM65.
- SA_DQS#4:** Connected to U19C pin AV57.
- SA_DQS#5:** Connected to U19C pin AV53.
- SA_DQS#6:** Connected to U19C pin AL43.
- SA_DQS#7:** Connected to U19C pin AL48.
- SA_DQS#8:** Connected to U19C pin AJ62.
- SA_DQS#9:** Connected to U19C pin AN61.
- SA_DQS#10:** Connected to U19C pin AN58.
- SA_DQS#11:** Connected to U19C pin AN55.
- SA_DQS#12:** Connected to U19C pin AW57.
- SA_DQS#13:** Connected to U19C pin AW53.
- SA_DQS#14:** Connected to U19C pin AL42.
- SA_DQS#15:** Connected to U19C pin AL49.
- SA_DQS#16:** Connected to U19C pin AU36.
- SA_DQS#17:** Connected to U19C pin AY37.
- SA_DQS#18:** Connected to U19C pin AR38.
- SA_DQS#19:** Connected to U19C pin AP36.
- SA_DQS#20:** Connected to U19C pin AU39.
- SA_DQS#21:** Connected to U19C pin AR36.
- SA_DQS#22:** Connected to U19C pin AU40.
- SA_DQS#23:** Connected to U19C pin AW39.
- SA_DQS#24:** Connected to U19C pin AY39.
- SA_DQS#25:** Connected to U19C pin AU40.
- SA_DQS#26:** Connected to U19C pin AP35.
- SA_DQS#27:** Connected to U19C pin AU41.
- SA_DQS#28:** Connected to U19C pin AU41.
- SA_DQS#29:** Connected to U19C pin AR35.
- SA_DQS#30:** Connected to U19C pin AU42.
- SA_DQS#31:** Connected to U19C pin AU42.
- SA_DQS#32:** Connected to U19C pin AU42.
- SA_DQS#33:** Connected to U19C pin AU42.
- SA_DQS#34:** Connected to U19C pin AU42.
- SA_DQS#35:** Connected to U19C pin AU42.
- SA_DQS#36:** Connected to U19C pin AU42.
- SA_DQS#37:** Connected to U19C pin AU42.
- SA_DQS#38:** Connected to U19C pin AU42.
- SA_DQS#39:** Connected to U19C pin AU42.
- SA_DQS#40:** Connected to U19C pin AU42.
- SA_DQS#41:** Connected to U19C pin AU42.
- SA_DQS#42:** Connected to U19C pin AU42.
- SA_DQS#43:** Connected to U19C pin AU42.
- SA_DQS#44:** Connected to U19C pin AU42.
- SA_DQS#45:** Connected to U19C pin AU42.
- SA_DQS#46:** Connected to U19C pin AU42.
- SA_DQS#47:** Connected to U19C pin AU42.
- SA_DQS#48:** Connected to U19C pin AU42.
- SA_DQS#49:** Connected to U19C pin AU42.
- SA_DQS#50:** Connected to U19C pin AU42.
- SA_DQS#51:** Connected to U19C pin AU42.
- SA_DQS#52:** Connected to U19C pin AU42.
- SA_DQS#53:** Connected to U19C pin AU42.
- SA_DQS#54:** Connected to U19C pin AU42.
- SA_DQS#55:** Connected to U19C pin AU42.
- SA_DQS#56:** Connected to U19C pin AU42.
- SA_DQS#57:** Connected to U19C pin AU42.
- SA_DQS#58:** Connected to U19C pin AU42.
- SA_DQS#59:** Connected to U19C pin AU42.
- SA_DQS#60:** Connected to U19C pin AU42.
- SA_DQS#61:** Connected to U19C pin AU42.
- SA_DQS#62:** Connected to U19C pin AU42.
- SA_DQS#63:** Connected to U19C pin AU42.
- SA_DQS#64:** Connected to U19C pin AU42.
- SA_DQS#65:** Connected to U19C pin AU42.
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- SA_DQS#72:** Connected to U19C pin AU42.
- SA_DQS#73:** Connected to U19C pin AU42.
- SA_DQS#74:** Connected to U19C pin AU42.
- SA_DQS#75:** Connected to U19C pin AU42.
- SA_DQS#76:** Connected to U19C pin AU42.
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- SA_DQS#78:** Connected to U19C pin AU42.
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- SA_DQS#80:** Connected to U19C pin AU42.
- SA_DQS#81:** Connected to U19C pin AU42.
- SA_DQS#82:** Connected to U19C pin AU42.
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- SA_DQS#92:** Connected to U19C pin AU42.
- SA_DQS#93:** Connected to U19C pin AU42.
- SA_DQS#94:** Connected to U19C pin AU42.
- SA_DQS#95:** Connected to U19C pin AU42.
- SA_DQS#96:** Connected to U19C pin AU42.
- SA_DQS#97:** Connected to U19C pin AU42.
- SA_DQS#98:** Connected to U19C pin AU42.
- SA_DQS#99:** Connected to U19C pin AU42.
- SA_DQS#100:** Connected to U19C pin AU42.
- SA_DQS#101:** Connected to U19C pin AU42.
- SA_DQS#102:** Connected to U19C pin AU42.
- SA_DQS#103:** Connected to U19C pin AU42.
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- SA_DQS#108:** Connected to U19C pin AU42.
- SA_DQS#109:** Connected to U19C pin AU42.
- SA_DQS#110:** Connected to U19C pin AU42.
- SA_DQS#111:** Connected to U19C pin AU42.
- SA_DQS#112:** Connected to U19C pin AU42.
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- SA_DQS#117:** Connected to U19C pin AU42.
- SA_DQS#118:** Connected to U19C pin AU42.
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- SA_DQS#128:** Connected to U19C pin AU42.
- SA_DQS#129:** Connected to U19C pin AU42.
- SA_DQS#130:** Connected to U19C pin AU42.
- SA_DQS#131:** Connected to U19C pin AU42.
- SA_DQS#132:** Connected to U19C pin AU42.
- SA_DQS#133:** Connected to U19C pin AU42.

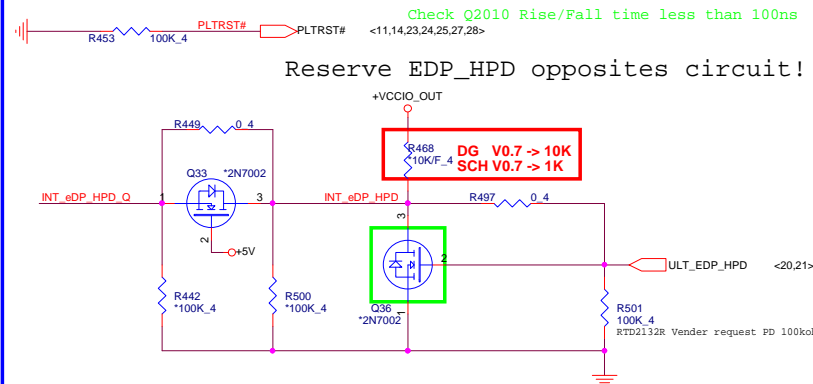




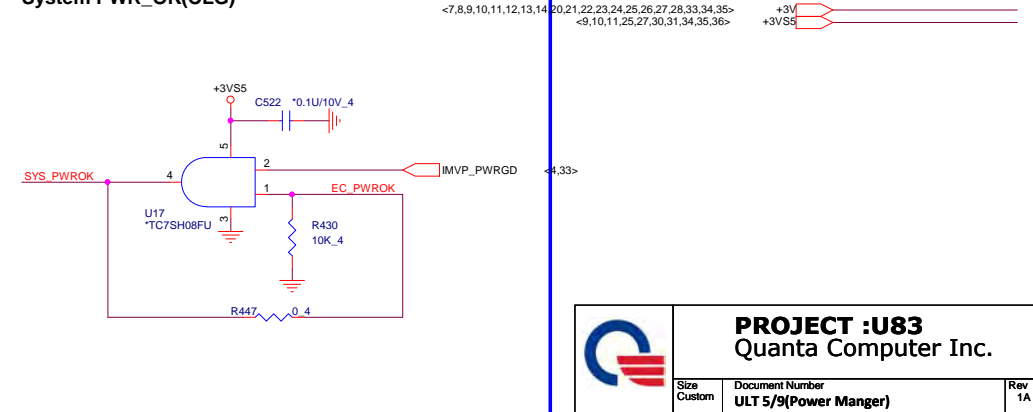
PCH Pull-high/low(CLG)



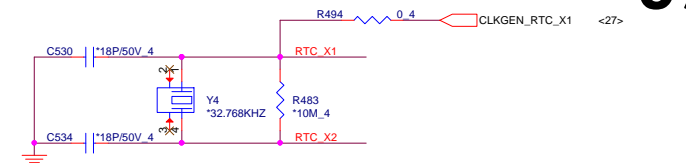
PLTRST#(CLG)



System PWR_OK(CLG)



07

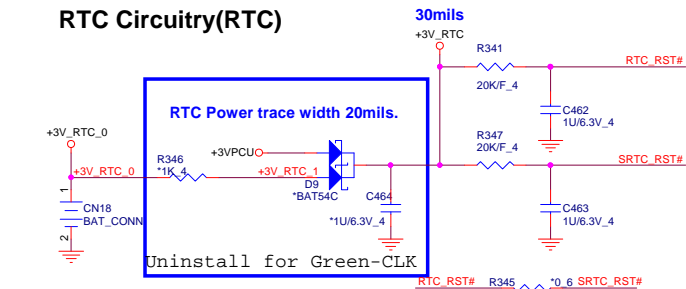


no stuff If use green Clock

HDD0 (SATA3 6.0Gb/s)

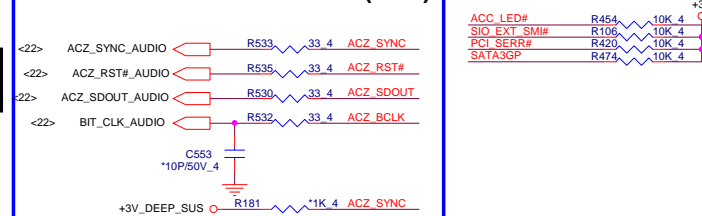
mSATA (SATA4 6Gb/s)

ODD (SATA3 6.0Gb/s)



HDA Bus(CLG)

GPIO Pull UP

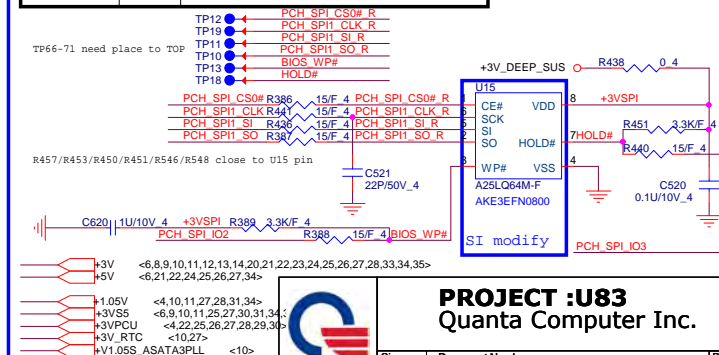


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden							
GPIO0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1"><thead><tr><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></tbody></table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up							

☐ PCH SPI ROM(CLG)

Vender	Size	P/N
AMIC	8MB	AKE3EFN0800 (A25LQ64M-F)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

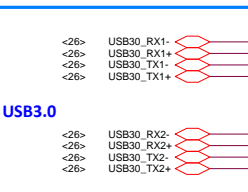
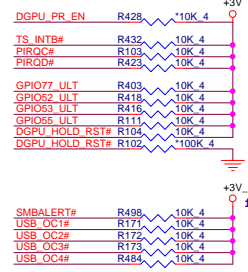


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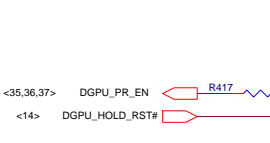
Size Custom	Document Number ULT 6/9(SATA/HDA)	Rev 1
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Lynx Point-LP Platform Controller Hub
(HDA, JTAG, SATA)

PCI/USBOC# Pull-up(CLG)



20111130 Modify USB3.0 for HM70



Cardreader

WLAN

LAN

USB2.0(M/B-1) (USBP0)
USB2.0/USB3.0 COMBO 1st
USB2.0 Small board (USBP1)
USB2.0/USB3.0 COMBO 2nd

Camera (USBP2)

USB2.0(M/B-2) (USBP5)

WLAN

Touch Screen

Cardreader

SI modify

WLAN

LAN

VGA

SI modify

CLOCK SIGNALS

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

SMBus/Pull-up(CLG)

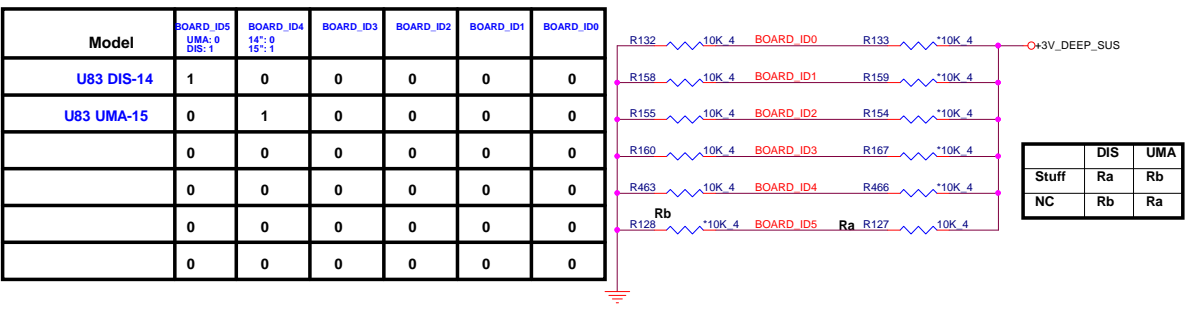
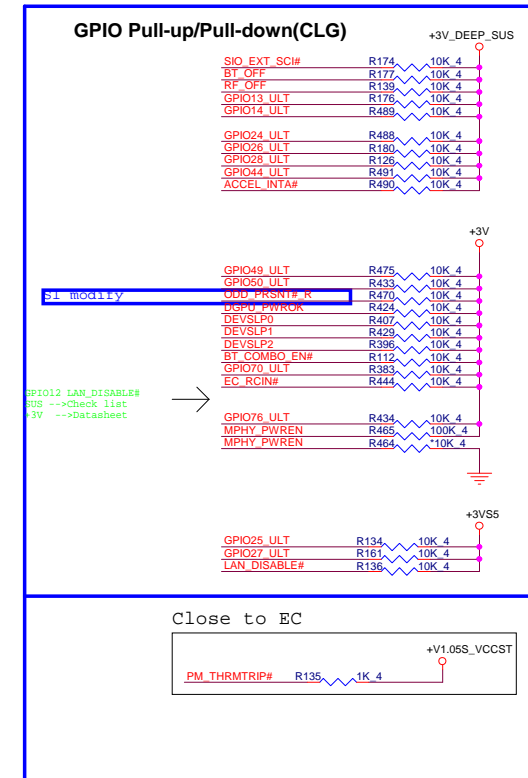
for D83




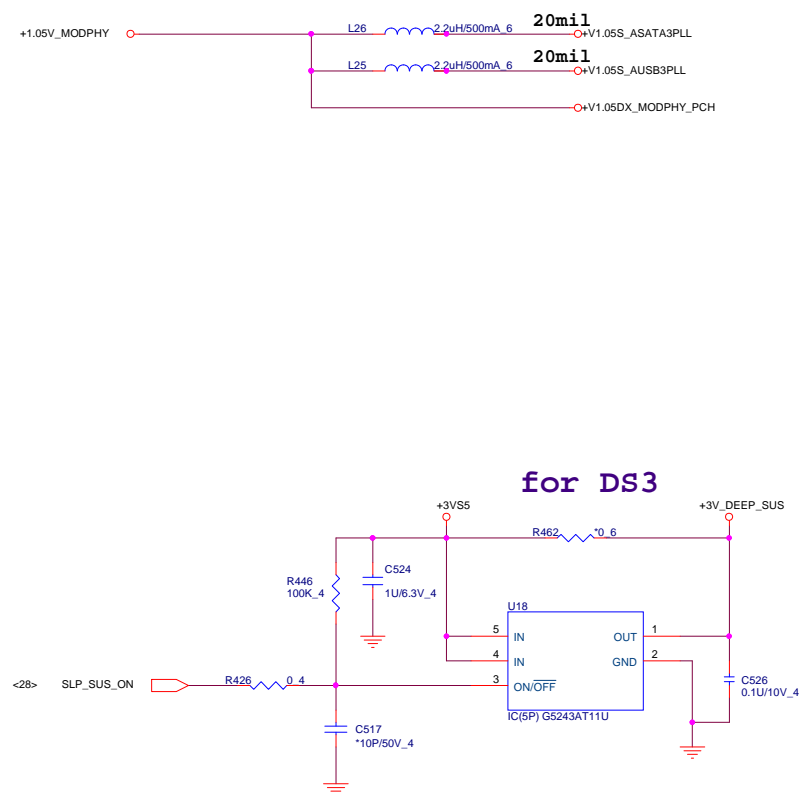
PROJECT :U83
Quanta Computer Inc.






















Size Custom	Document Number	Rev 1A
	ULT 7/9 (PCIe/USB/CLK)	
Date: Thursday, March 14, 2013	Sheet 8 of 41	

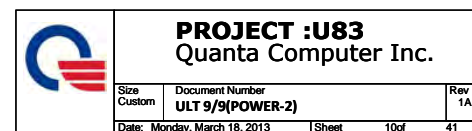
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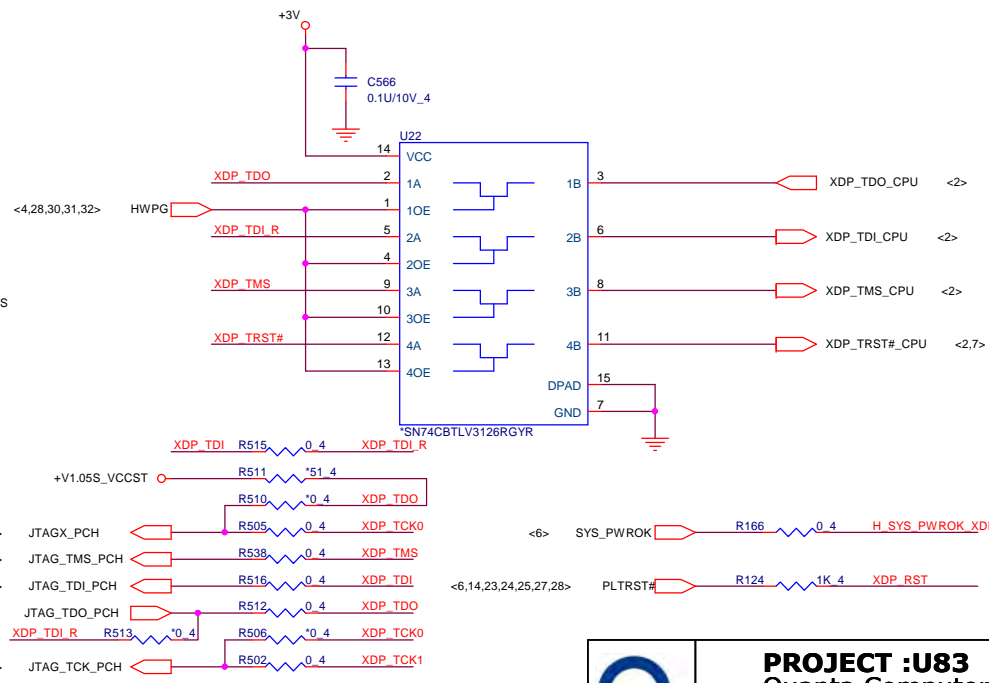
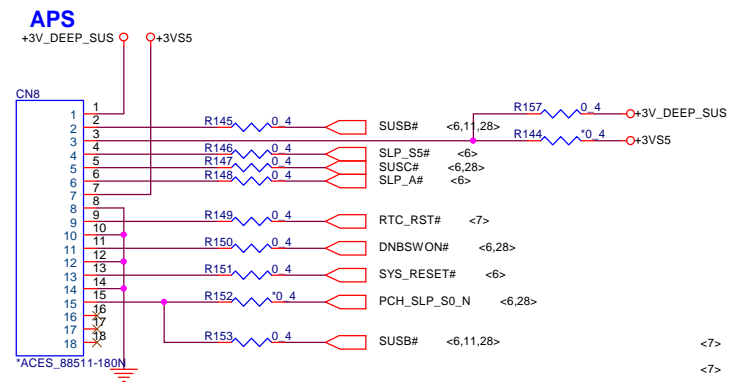
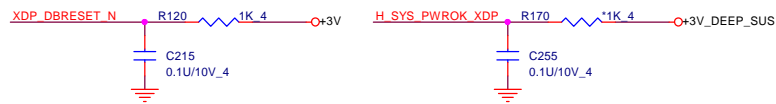
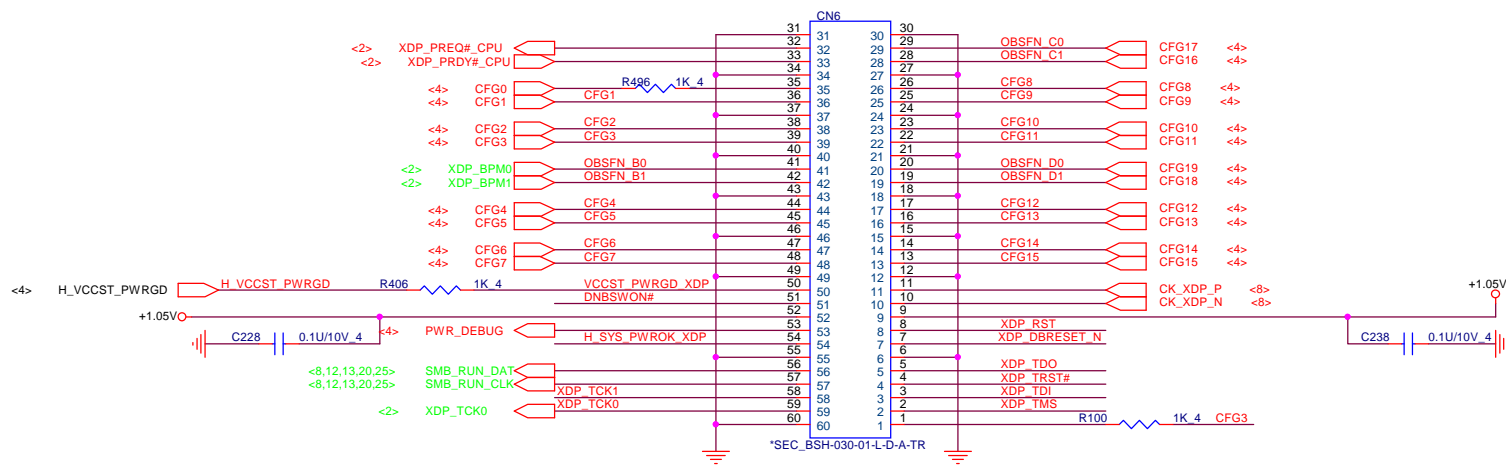


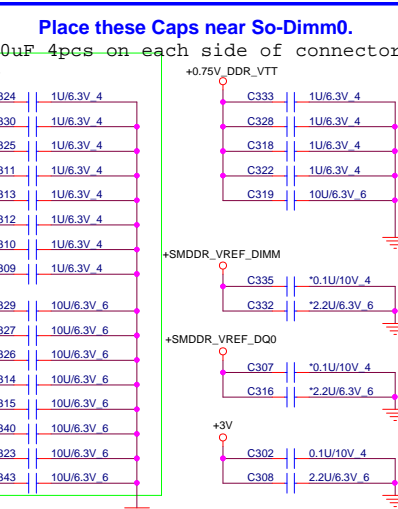
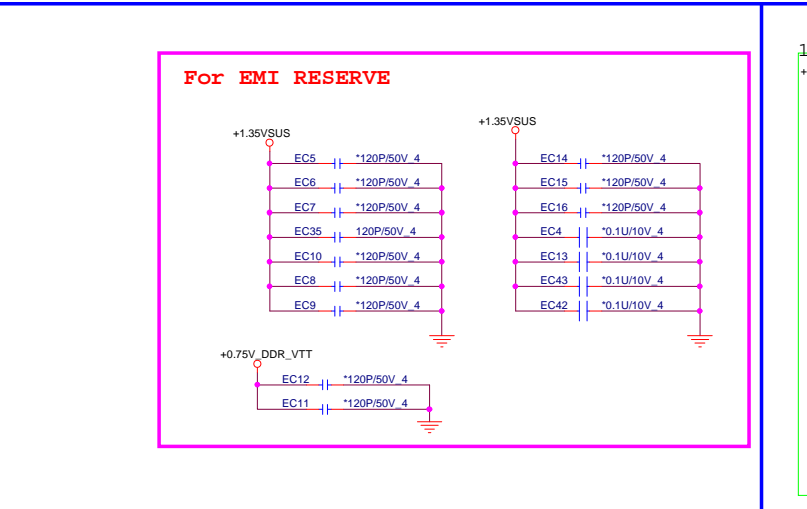
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	Size Custom	Document Number ULT 8/9 (GPIO/MISC)	Rev 1A
	Date: Thursday, March 14, 2013	Sheet	9 of 41

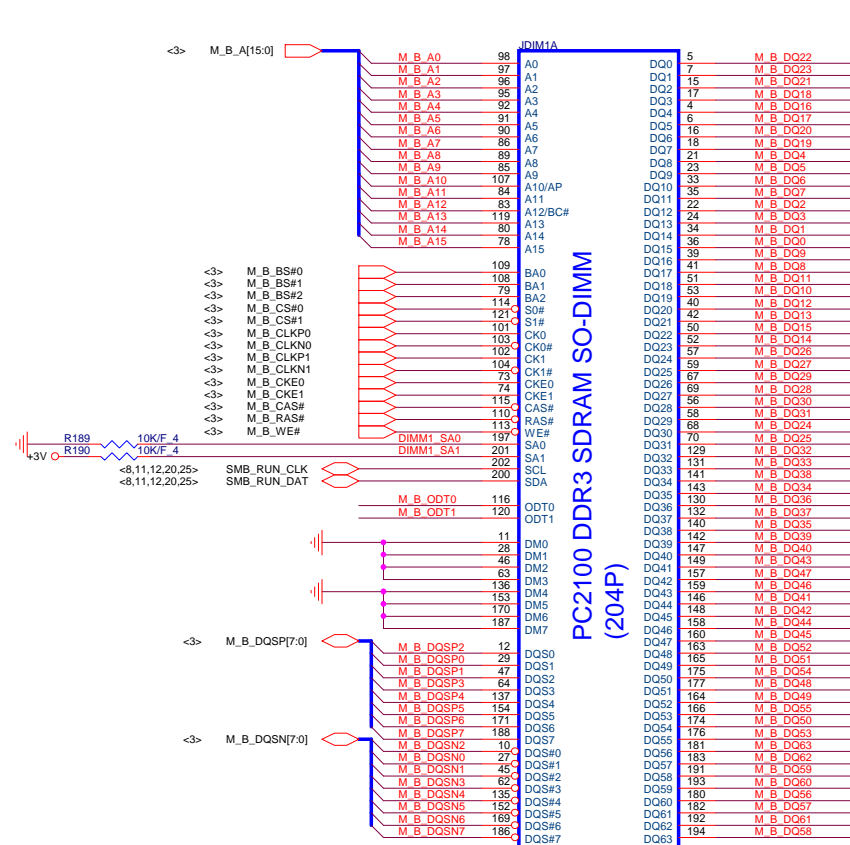


		<6,7,8,9,11,12,13,14,20,21,22,23,24,25,26,27,28,33,34,35>										+3V	
<6,21,22,24,25,26,27,34>		+5V			<8>	+V1.05S_AUSB3PLL			<7>	+V1.05S_ASATA3PLL			
<4,7,11,27,28,31,34>		+1.05V			<8>	+V1.05S_AXCK_LCPLL			<27>	+3V_RTC			
<6,9,11,25,27,30,31,34,35,36>		+3VS5			<2,4,12,13,25,32>				+1.35VSUS				
<13,22,25,26,30,32,33,34,35,36,37>		+5VS5											

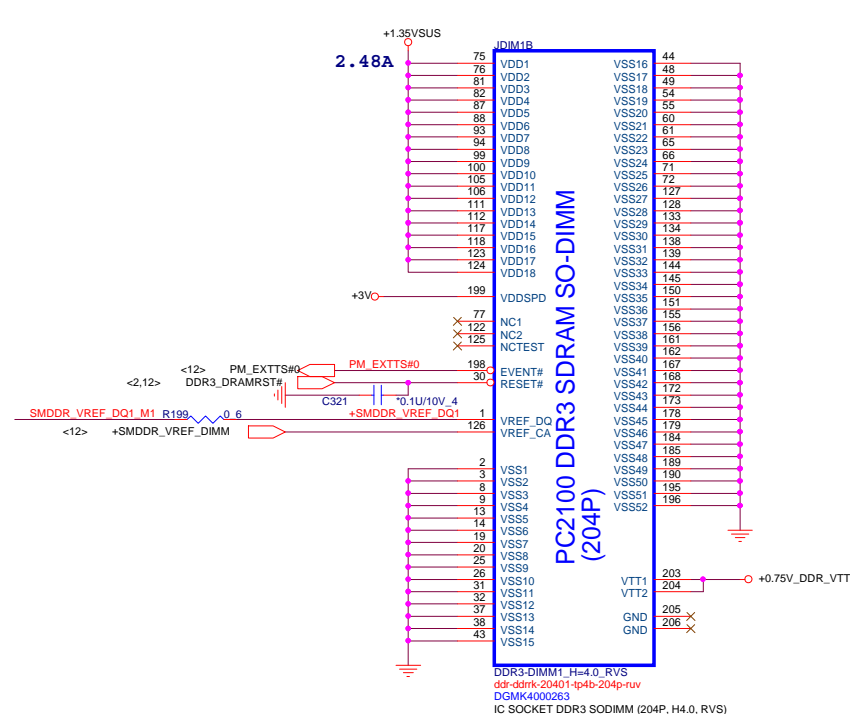






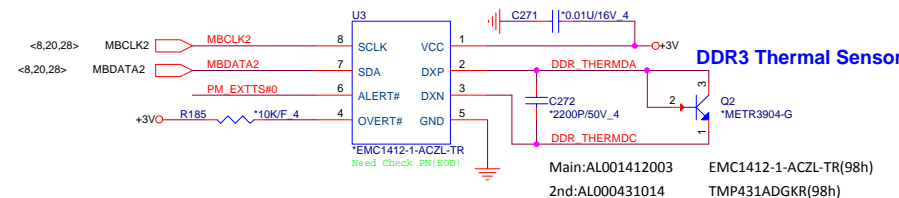


DDR3-DIMM1_H=4.0_RVS
ddr-ddr3k-20401-tp4b-204p-ruv
DGMK4000263
IC SOCKET DDR3 SODIMM (204P, H4.0, RVS)



DDR3-DIMM1_H=4.0_RVS
ddr-ddr3k-20401-tp4b-204p-ruv
DGMK4000263
IC SOCKET DDR3 SODIMM (204P, H4.0, RVS)

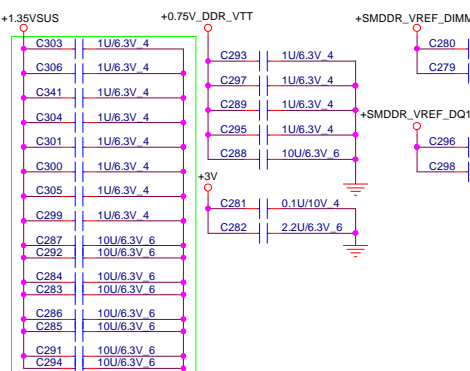
Local Thermal Sensor



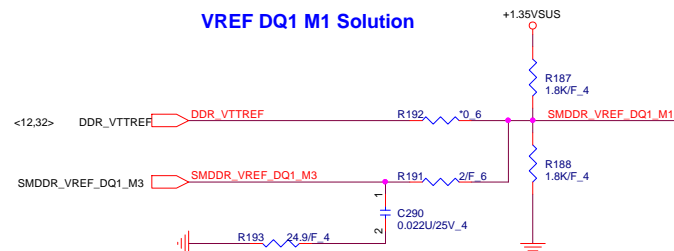
Main:AL001412003 EMC1412-1-ACZL-TR(96h)
2nd:AL000431014 TMP431ADGKR(96h)

Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector

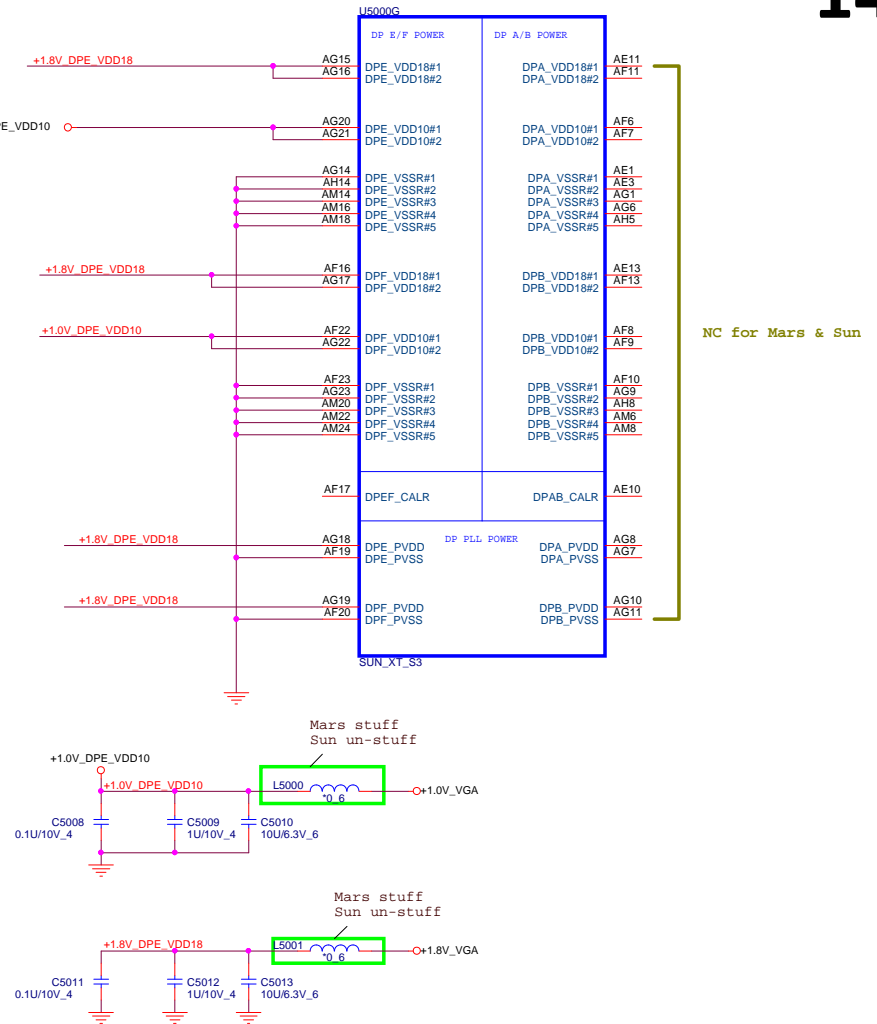
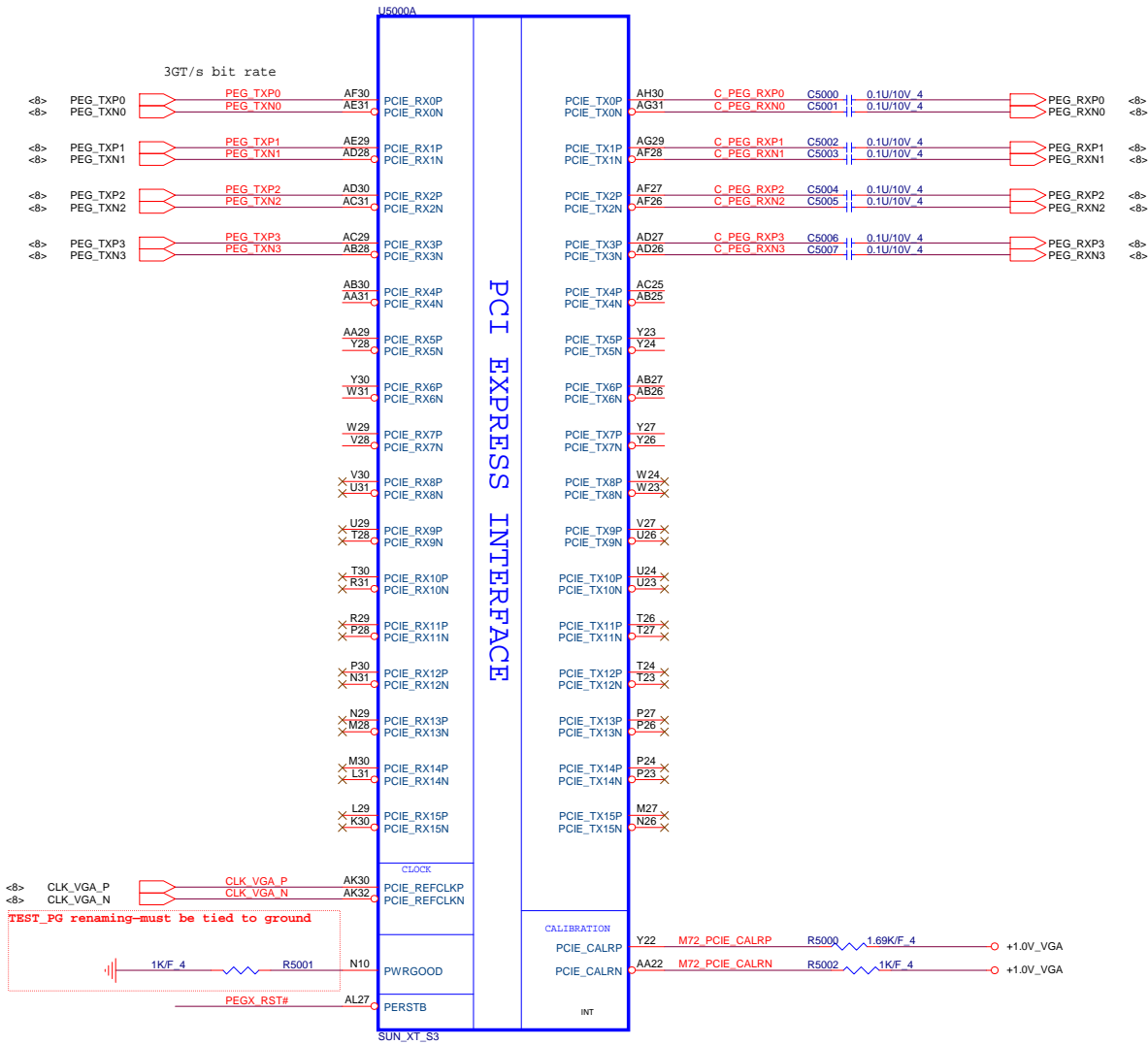


VREF DQ1 M1 Solution

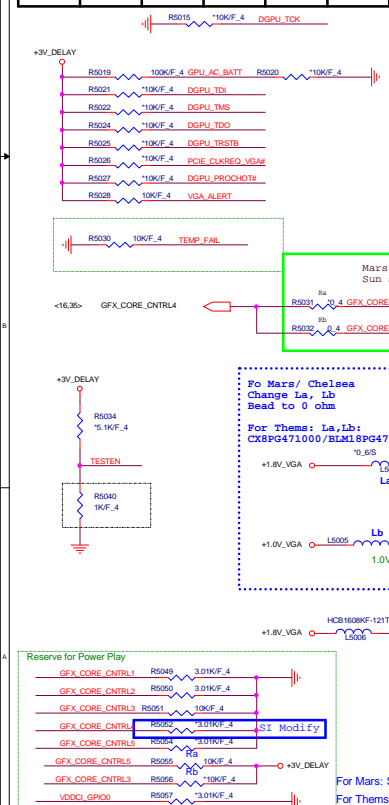


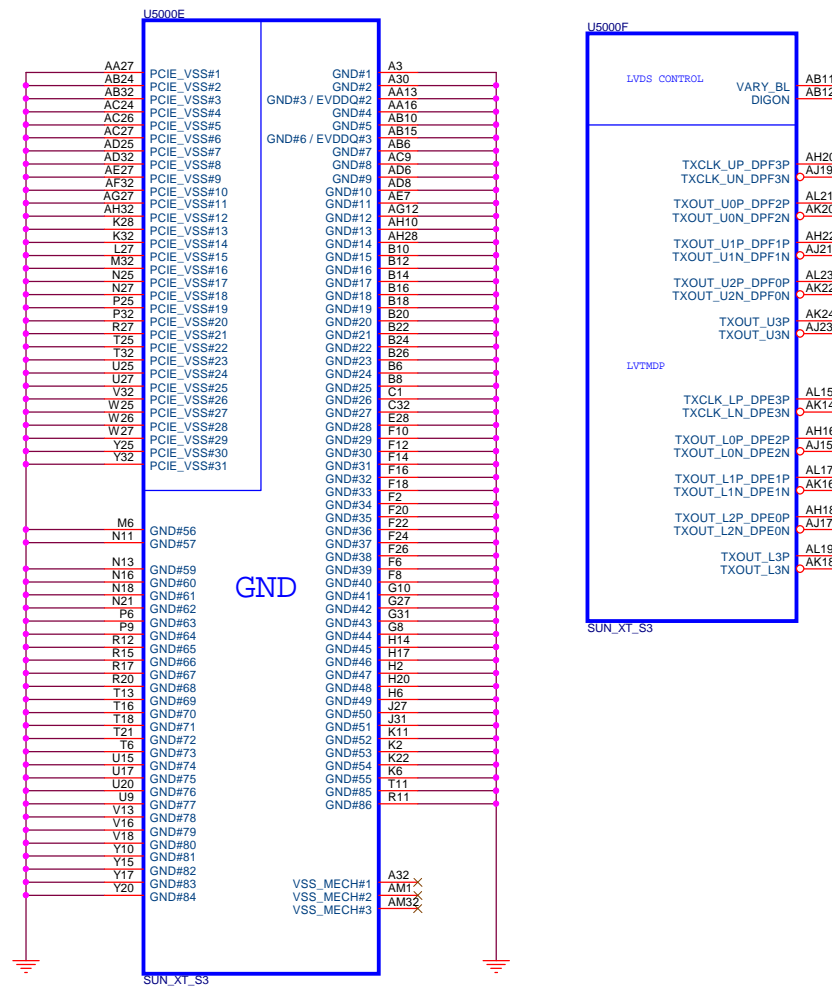
PROJECT :U83
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Custom	DDR3 DIMM1-RVS(4.0H)	1A
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GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT
PWRCTRL15	PWRCTRL14	PWRCTRL3	PWRCTRL2	PWRCTRL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	1	0	0.975V
1	0	1	1	1	0.950V
1	1	0	0	0	0.925V
1	1	0	0	1	0.900V
1	1	0	1	0	0.875V
1	1	0	1	1	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	1	0	0.775V





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

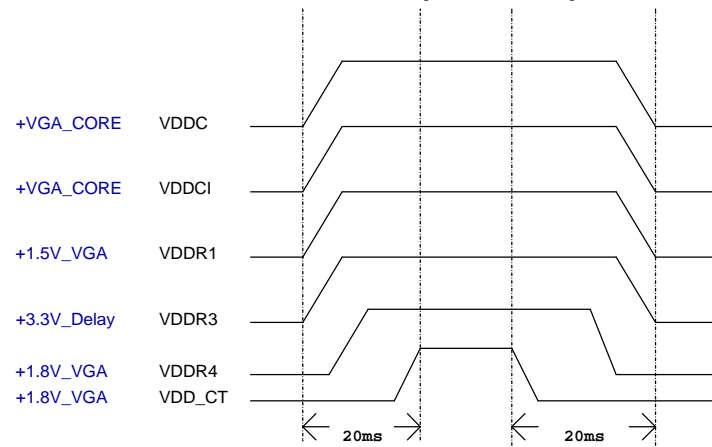
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIOQ[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

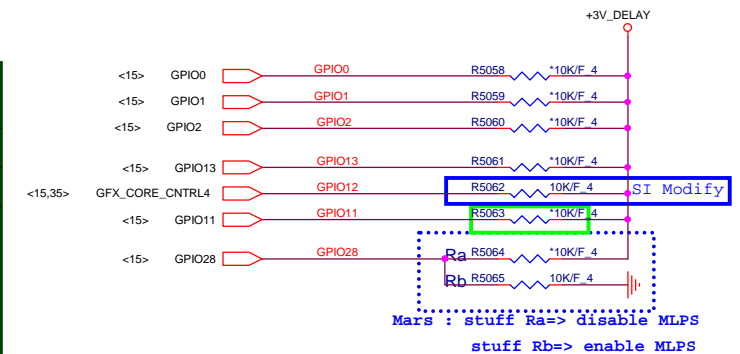
Power Up/Down Sequence



Memory Aperture size(Seymour)

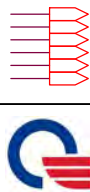
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

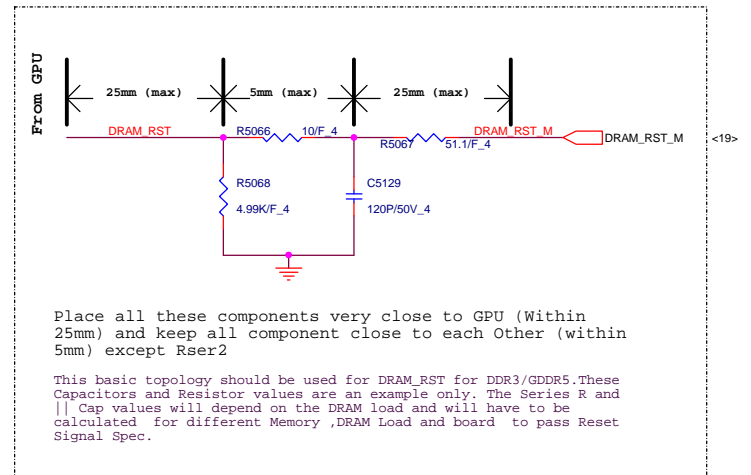
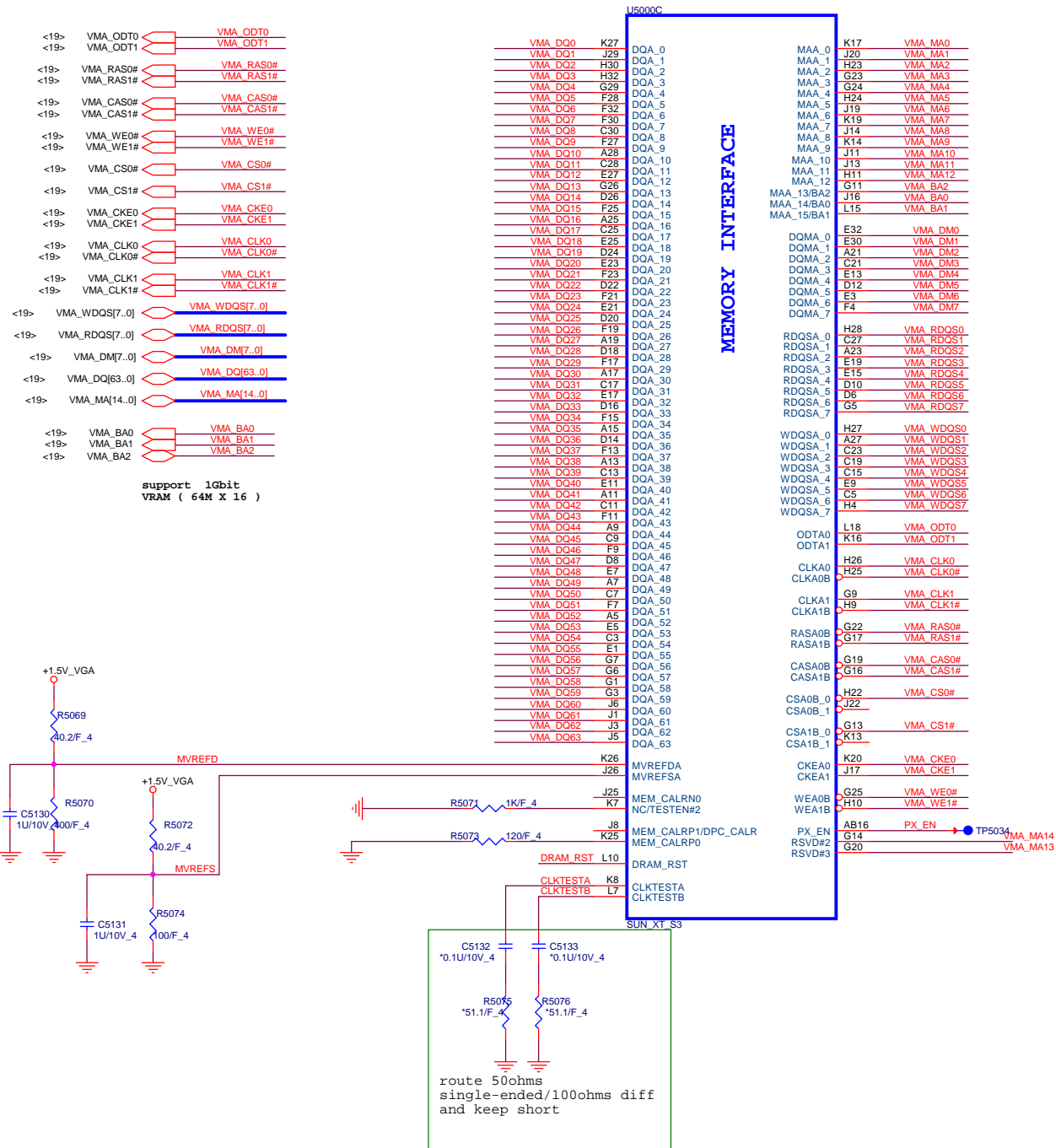


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Quanta Computer Inc.

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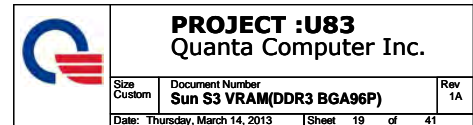


Size Custom	Document Number Sun S3 Power_and_NC	Rev 1A
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Quanta Computer Inc.

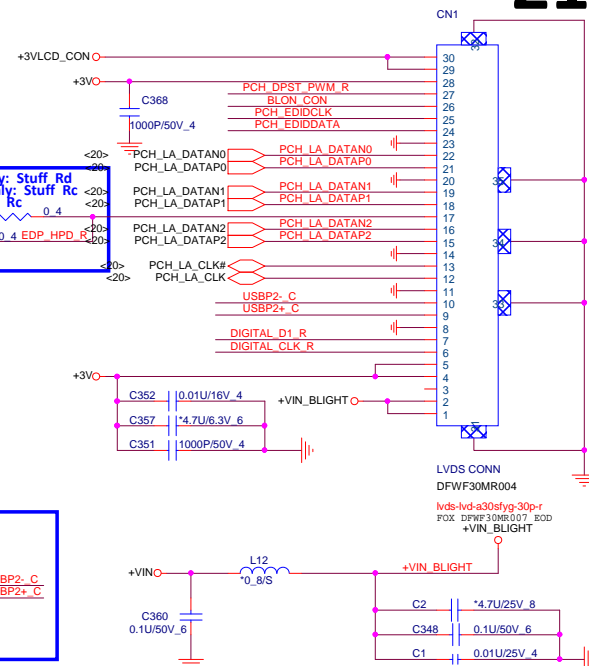
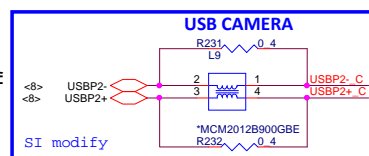
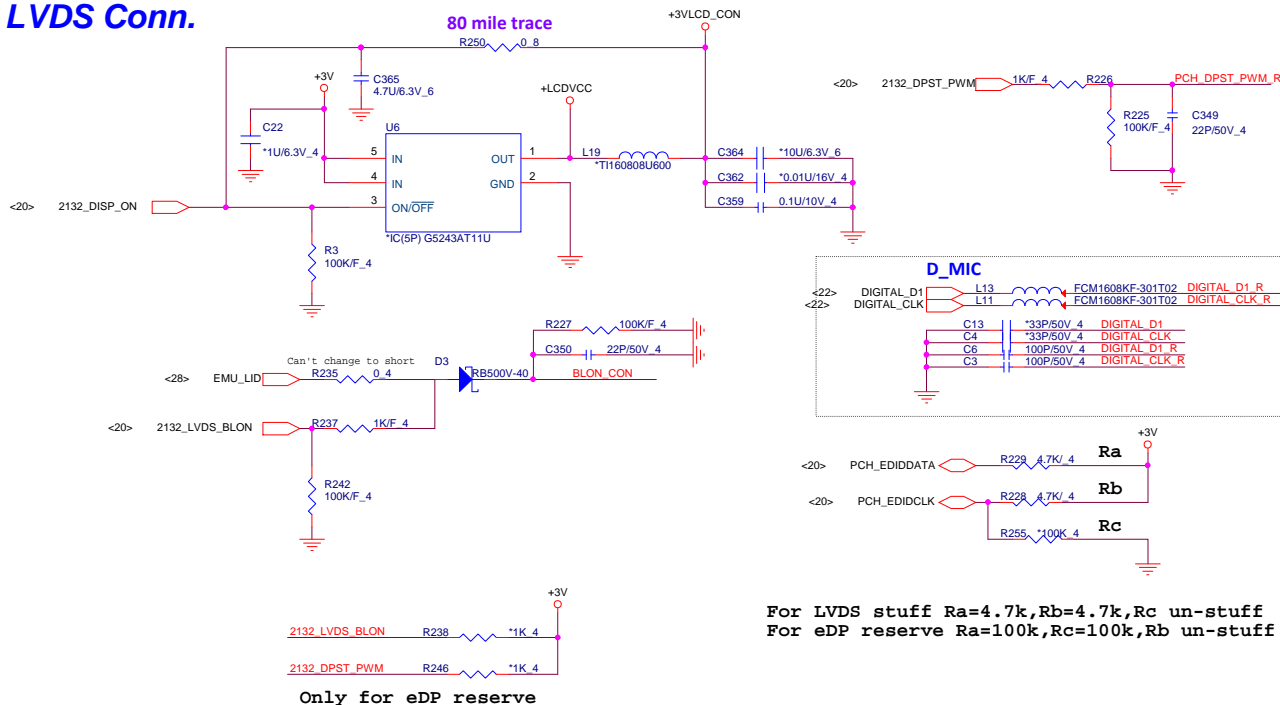
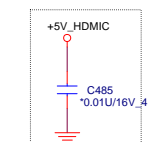
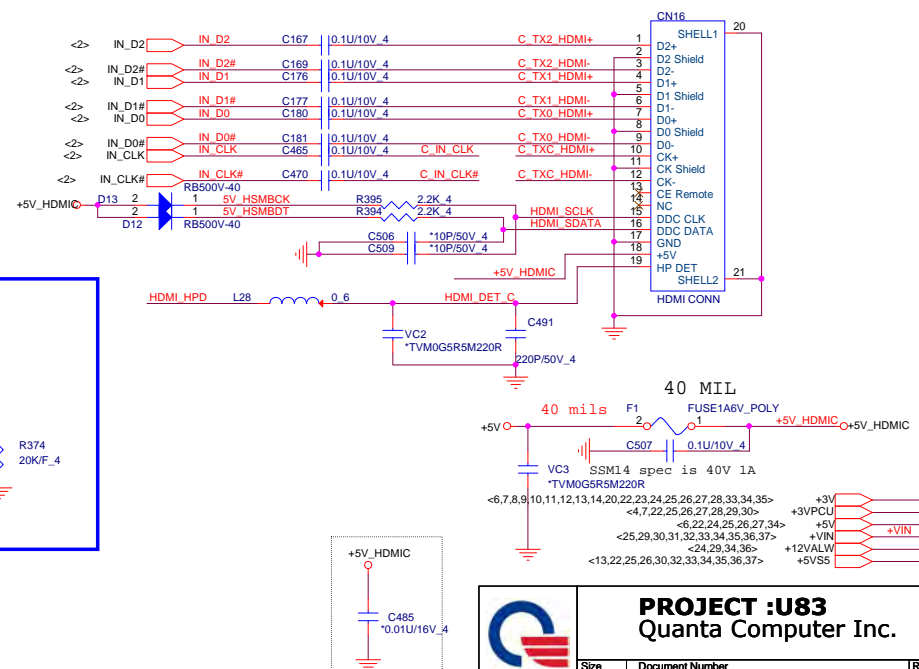
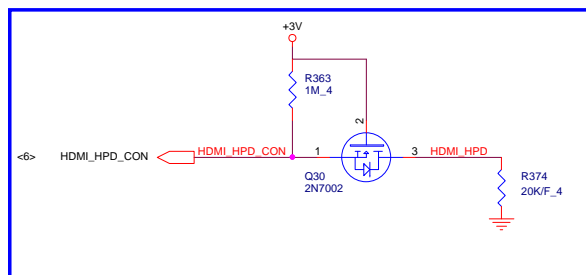
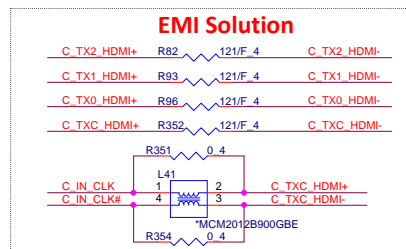
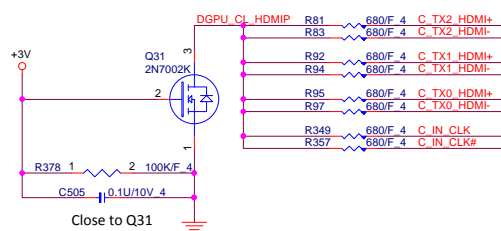
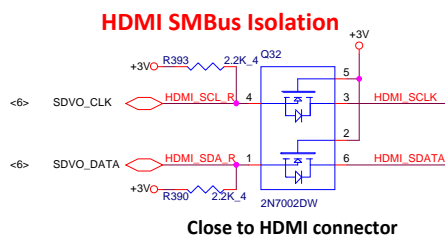
Size	Document Number	Rev
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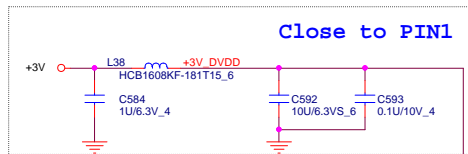
A

A

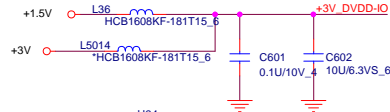
LVDS Conn.

**HDMI Conn.**

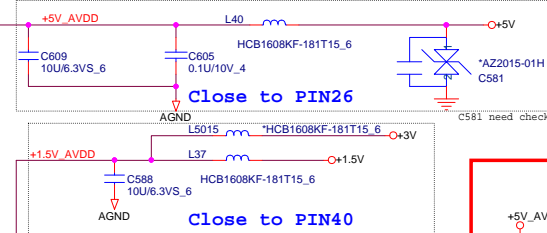
Close to PIN1



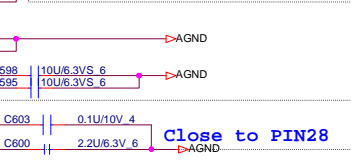
>40mils trace



Close to PIN26



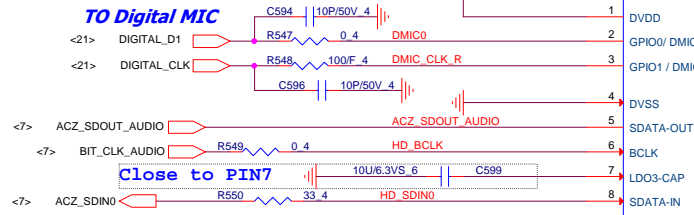
Close to PIN40



Close to PIN28

<6,7,8,9,10,11,12,13,14,20,21,23,24,25,26,27,28,33,34,35>
<10,25,27,31>+5V
+3V
+1.5V

TO Digital MIC

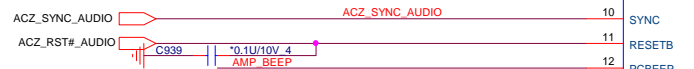


Close to PIN7



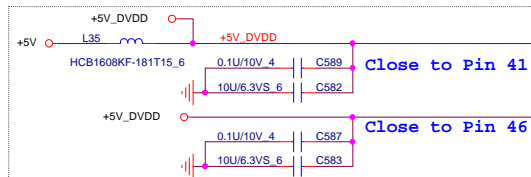
Analog

Digital

AVDD1
AVDD2
AVSS1
AVSS2
LDO1-CAP
LDO2-CAP
VREF
HPROUT-L (PORT I)
HPROUT-R (PORT I)
LINE2-L
LINE2-R
LINE1-L (PORTC)
LINE1-R (PORTC)
MIC1-R (PORTB)
MIC1-L (PORTB)
MIC1-VREFO-L
MIC1-VREFO-R
MIC2-R (PORTF)
MIC2-L (PORTF)
MIC2-VREFO
MONO-OUT
SenseA
SenseB
JOREF
ALC3227 x QFN48
SENSE A
COMBO GPI
R546
C585
4.7U/6.3V_6
AGND

Close to Pin 34,35,36

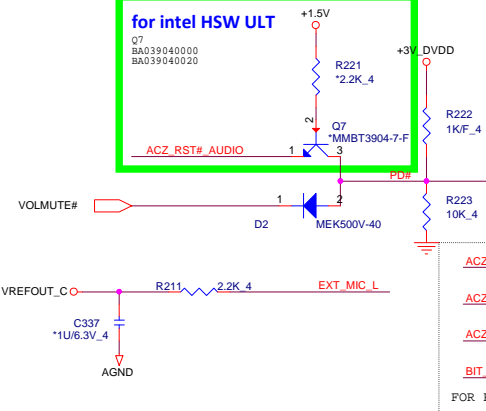
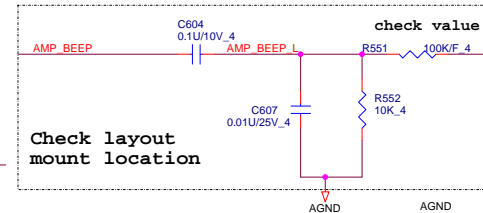
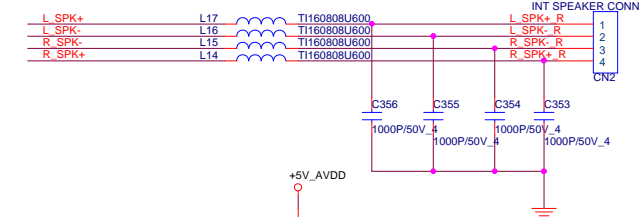
TO Internal Speakers



PD#

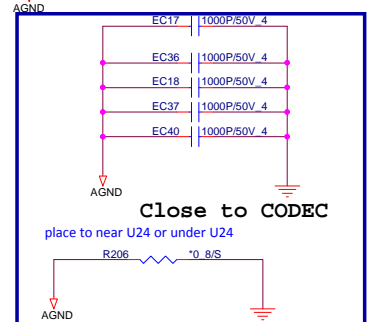
USB 2.0 AND AUDIO COMBO JACK

for intel HSW ULT

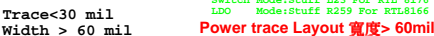
Check layout
mount locationClose to Speaker
Speaker 4 ohm: 40mils

Close to CODEC

place to near U24 or under U24

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Custom	Azalia ALC 3227	1A
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Place Cc,Cd,Ce,Cf
close to each VDD10 pin-- 3, 8, 22, 30

Place Cg & C621 close to each VDD10 pin22

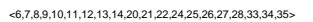
*RTL8166EH Cg & C621 close pin30



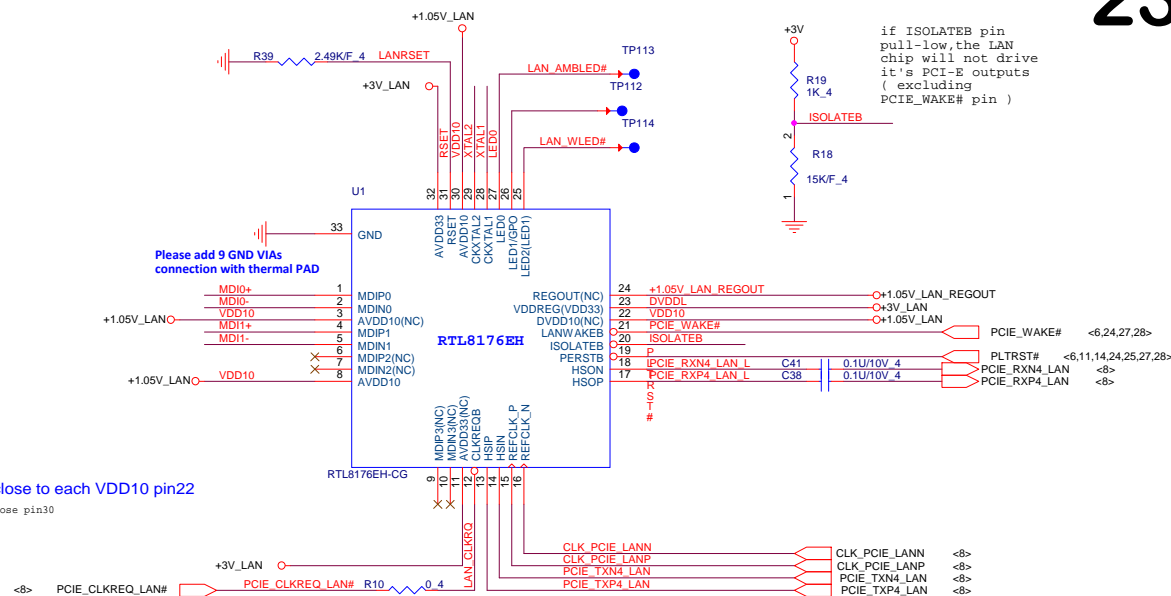
Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



Remove For Not Using SWR mode

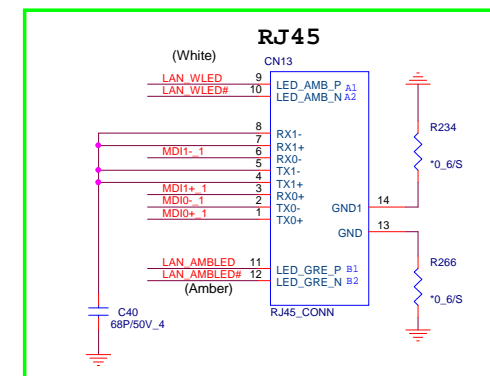


+3V



```
if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

TWD Type



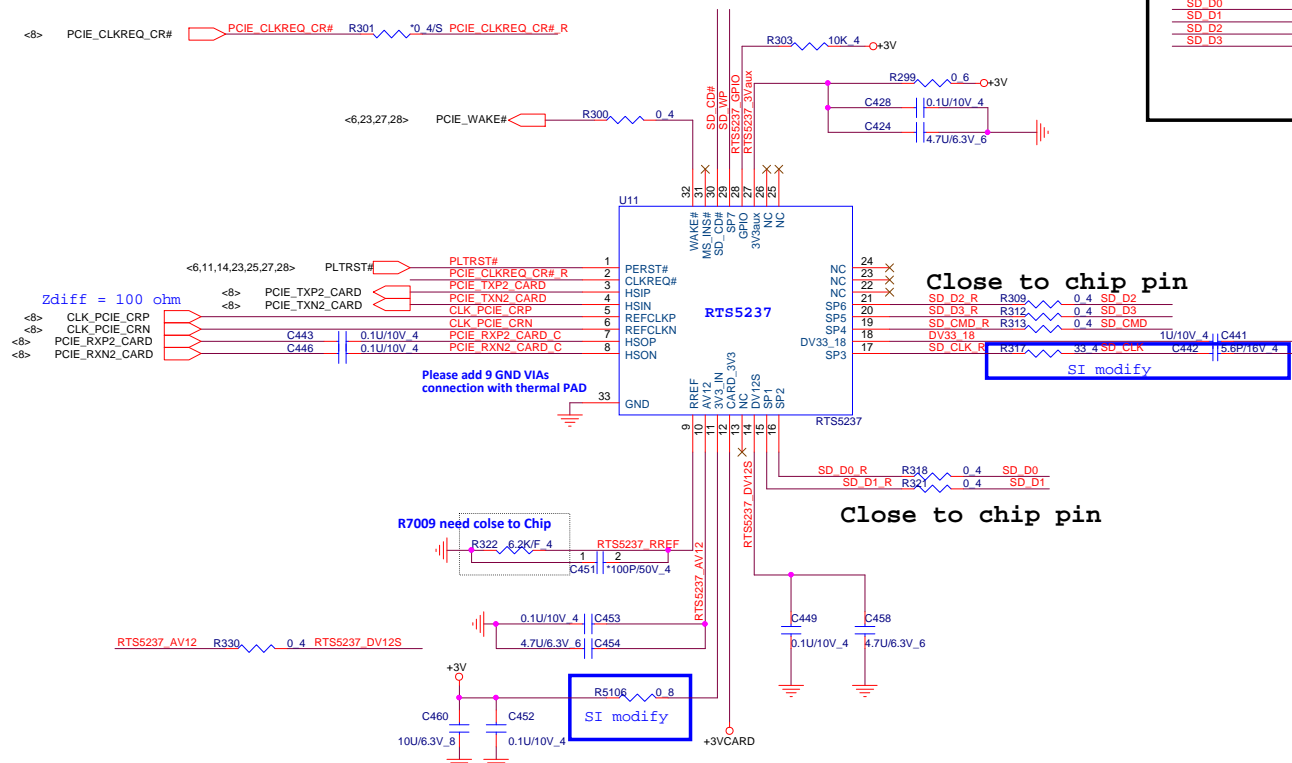
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SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK

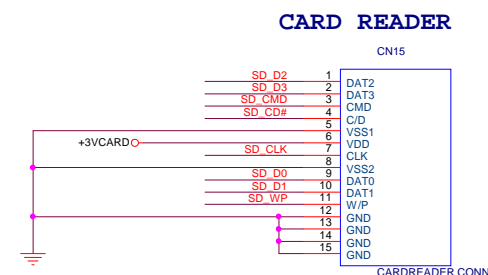
Share Pin

SD / MMC



Close to chip pin

CLOSE CONN

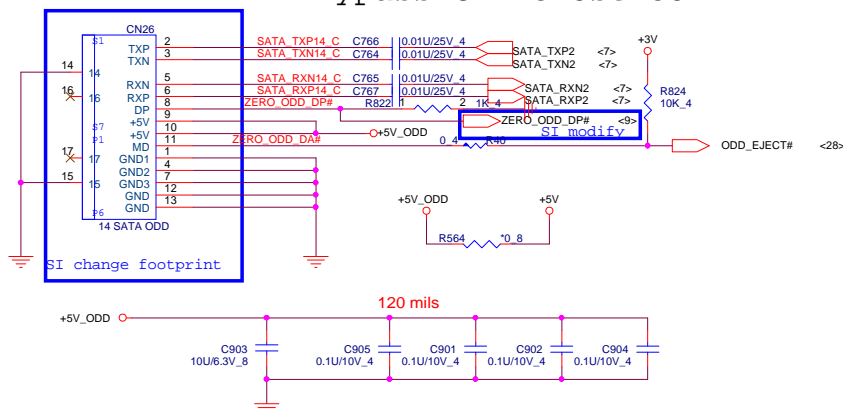


R3X Type

**SATA ODD
CONNECTOR**

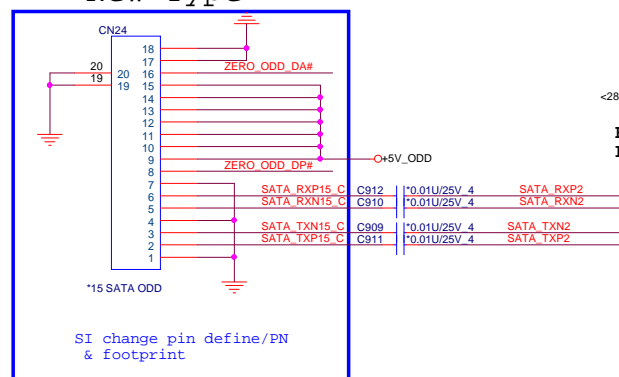
14" SATA ODD

Bypass CAP close conn

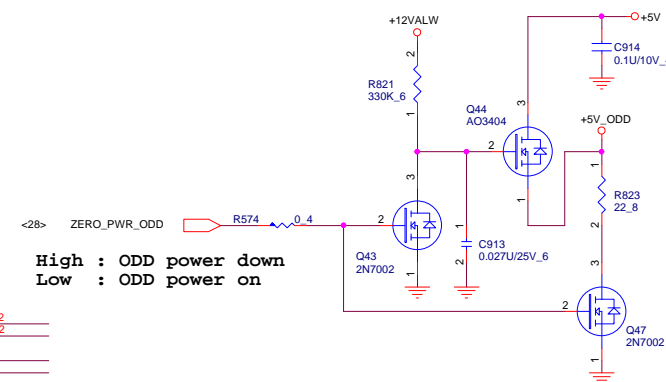


15" SATA ODD

New Type



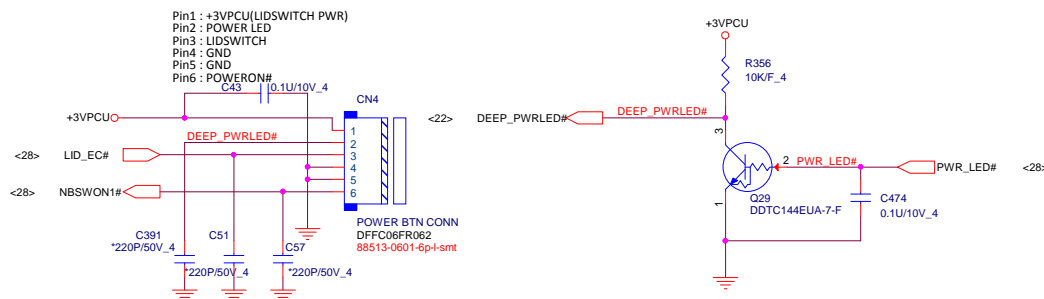
High : ODD power down
Low : ODD power on



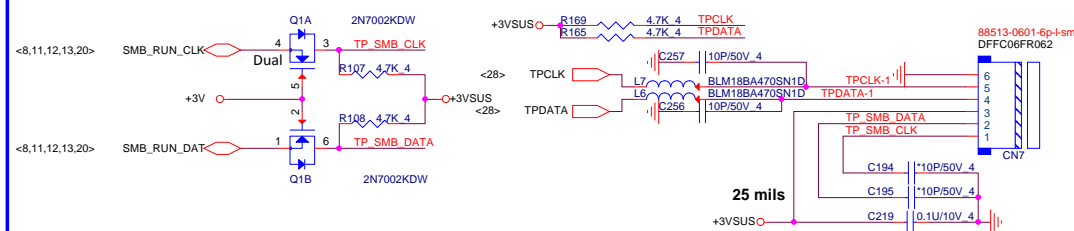
PROJECT :U83
Quanta Computer Inc.

Size Custom	Document Number CR RTS5237 & CR SOCKET	Rev 1.
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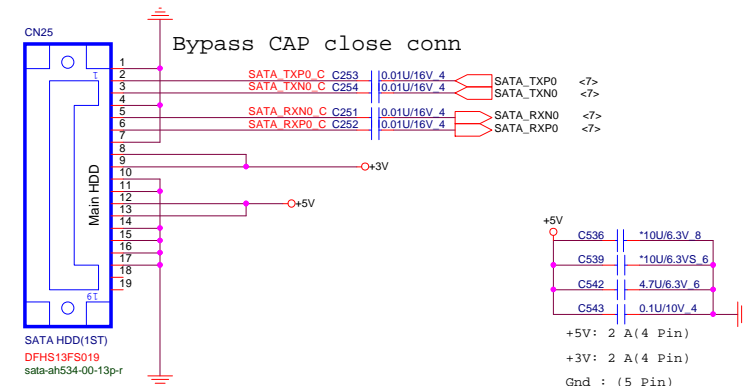
Power Botton Connector



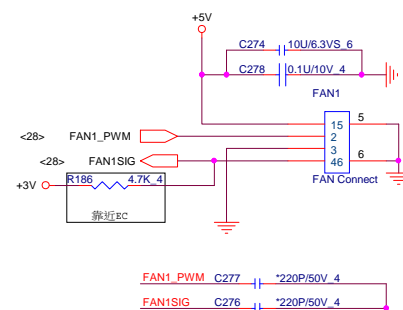
Touch Pad Connector



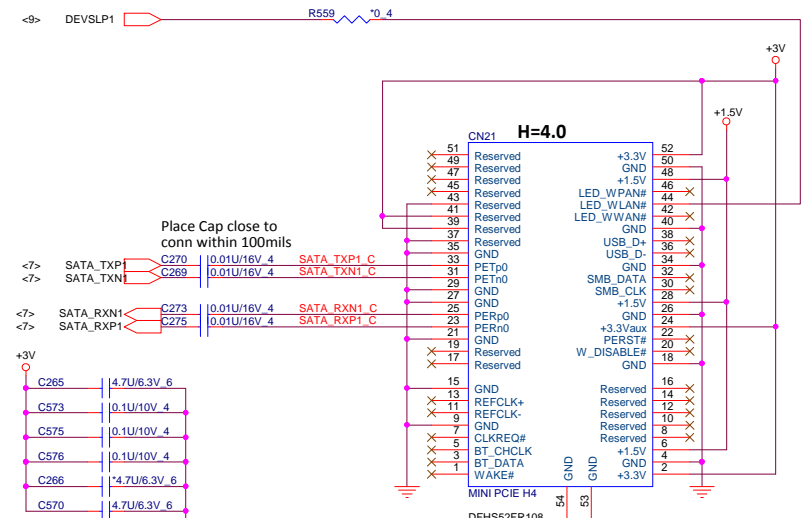
SATA HDD Connector(Cable type)



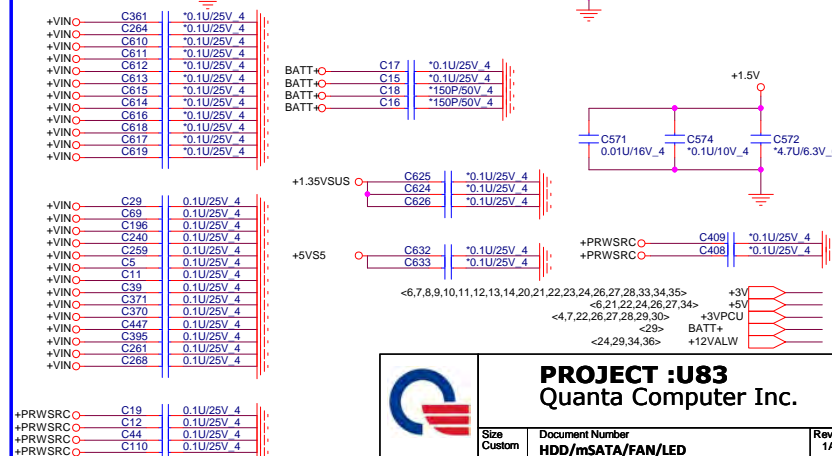
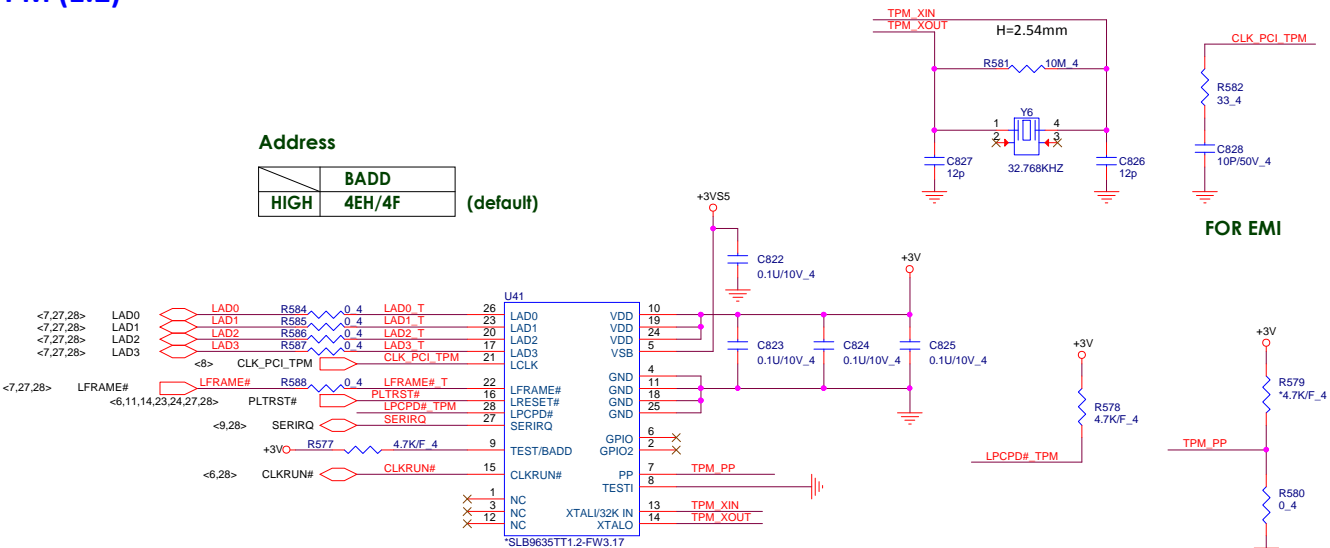
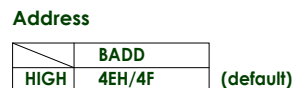
FAN



Mini PCI-E Card 2- Full size mSATA

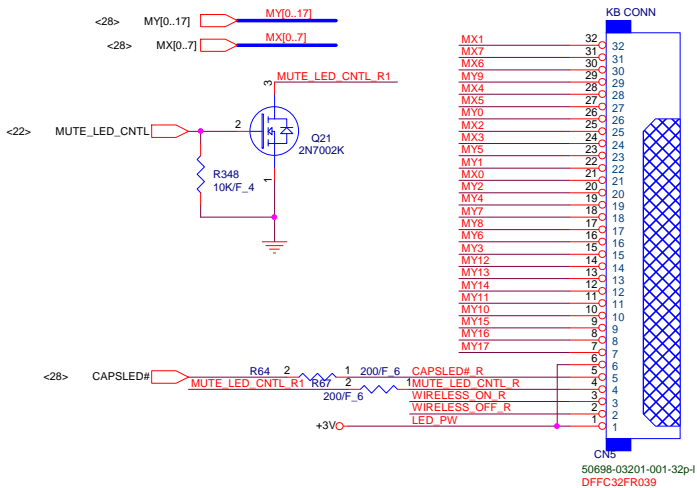


TPM (1.2)

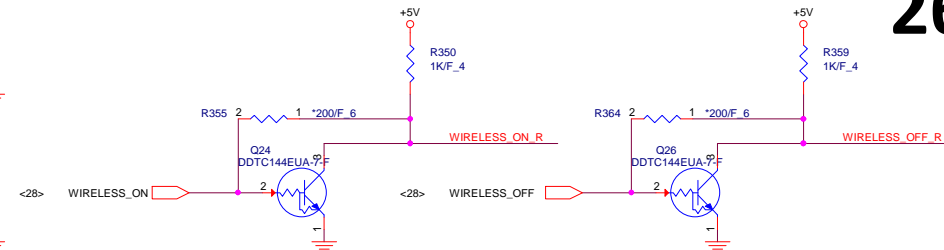
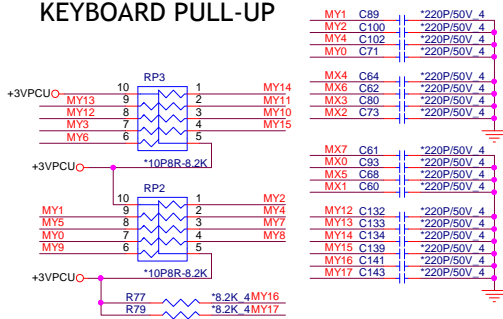


KEYBOARD Con.

26

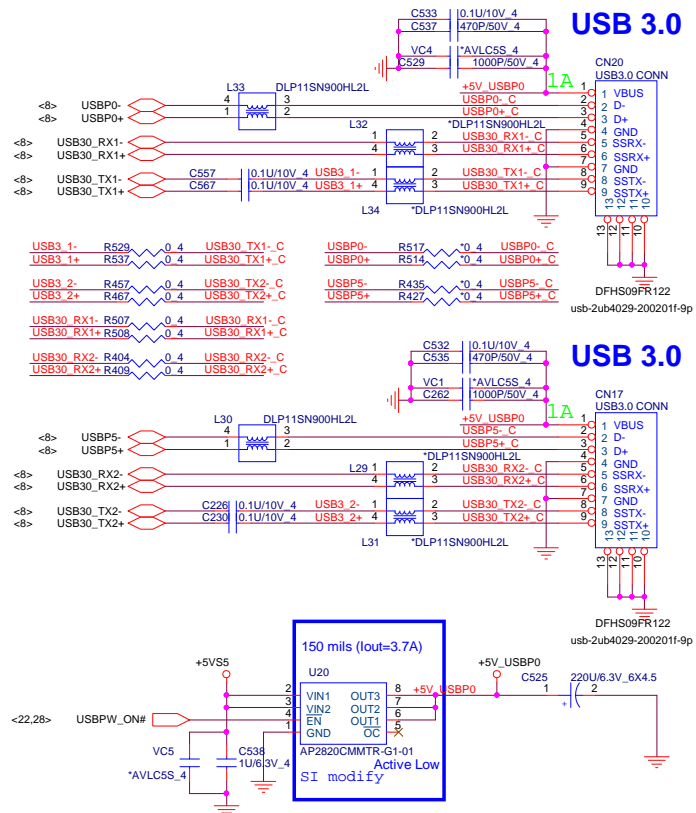
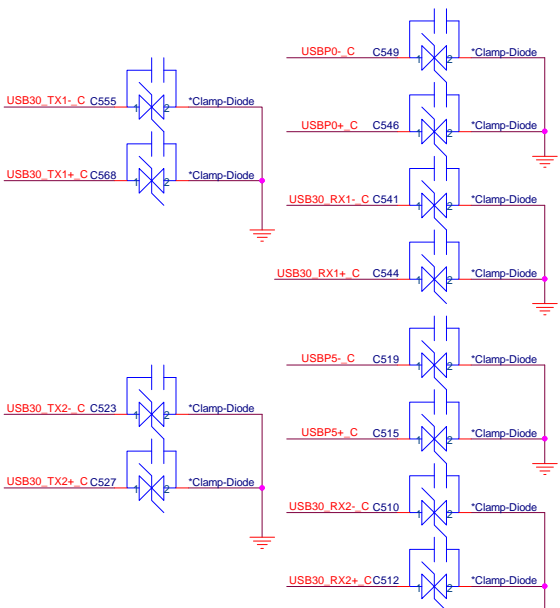


KEYBOARD PULL-UP

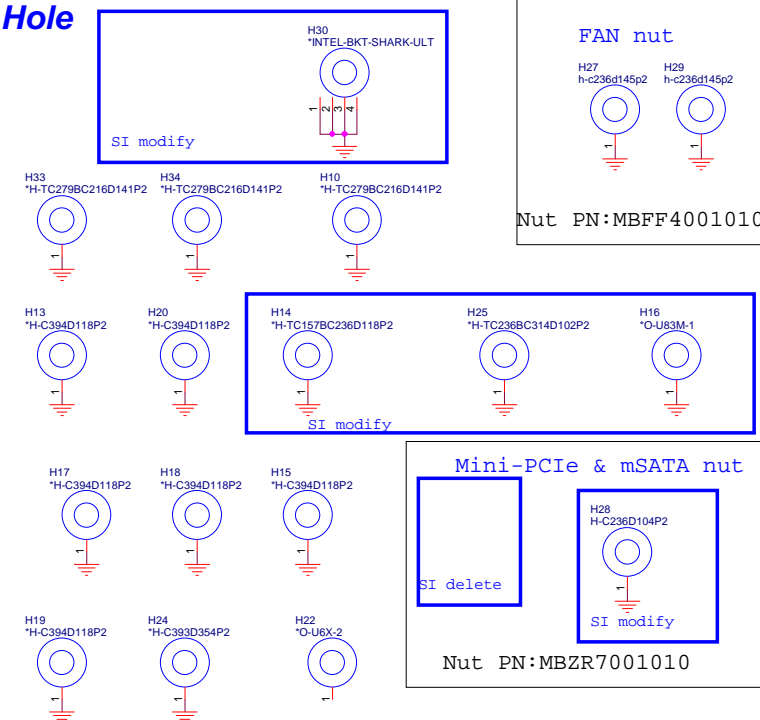


R6X Type

USB 2.0/3.0 Combo

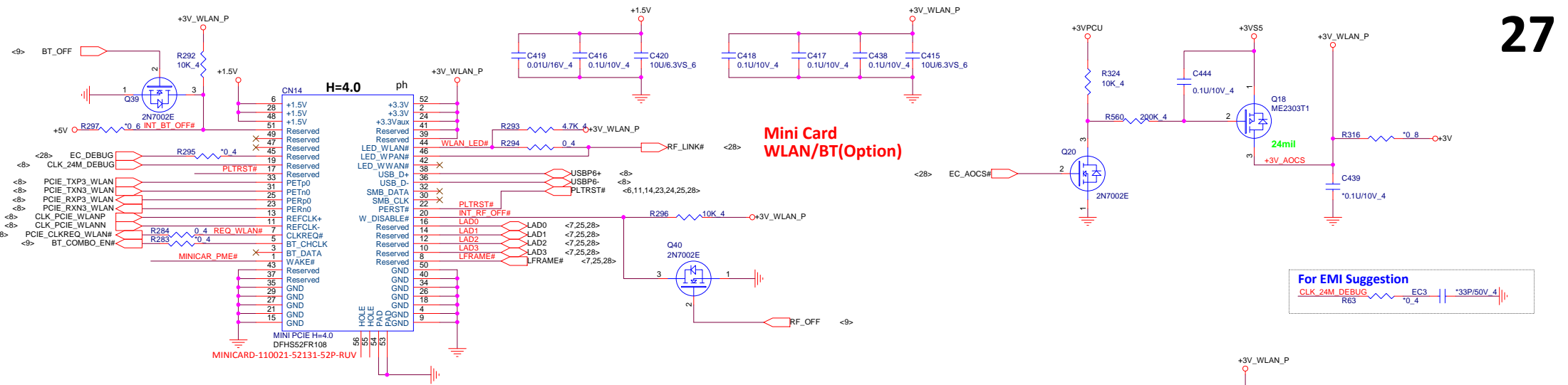


Hole

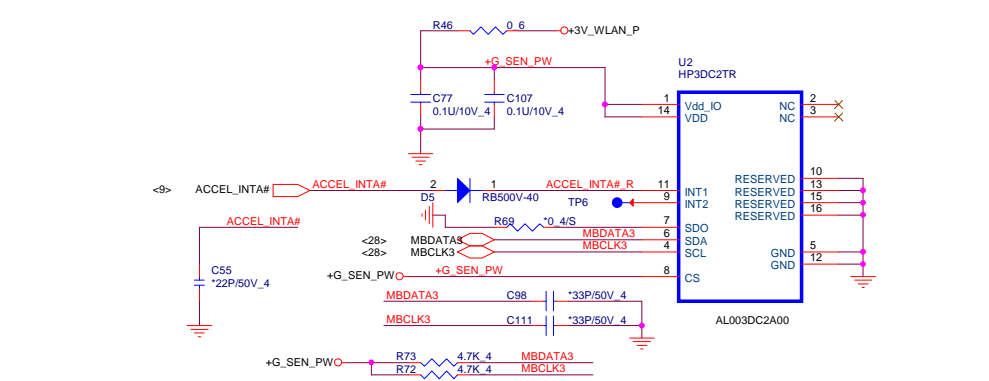


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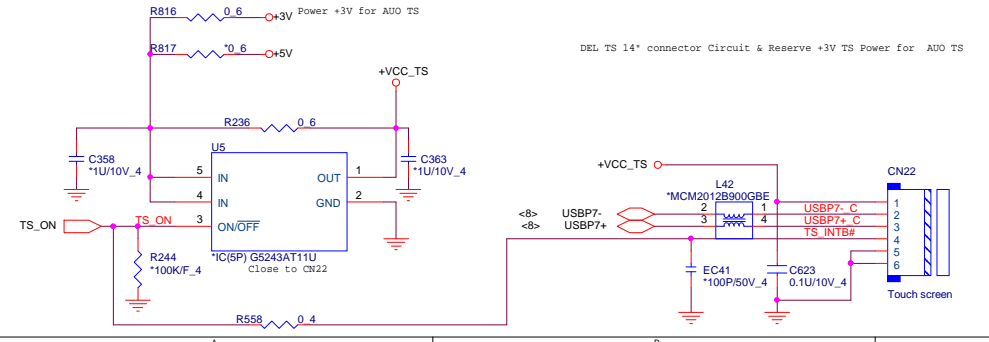
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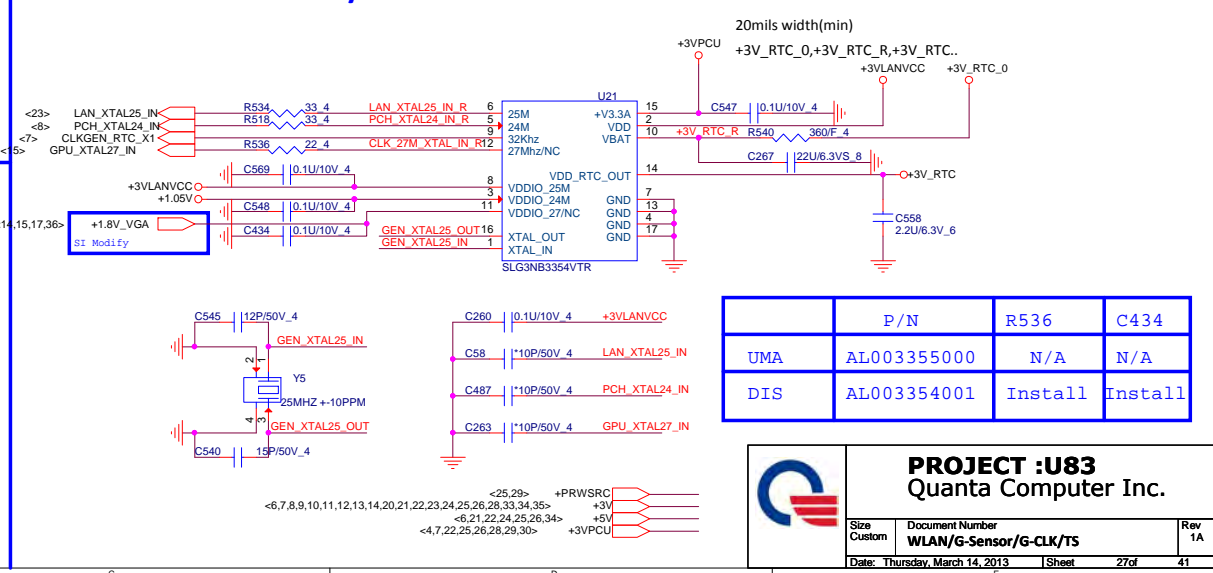
Accelerometer Sensor



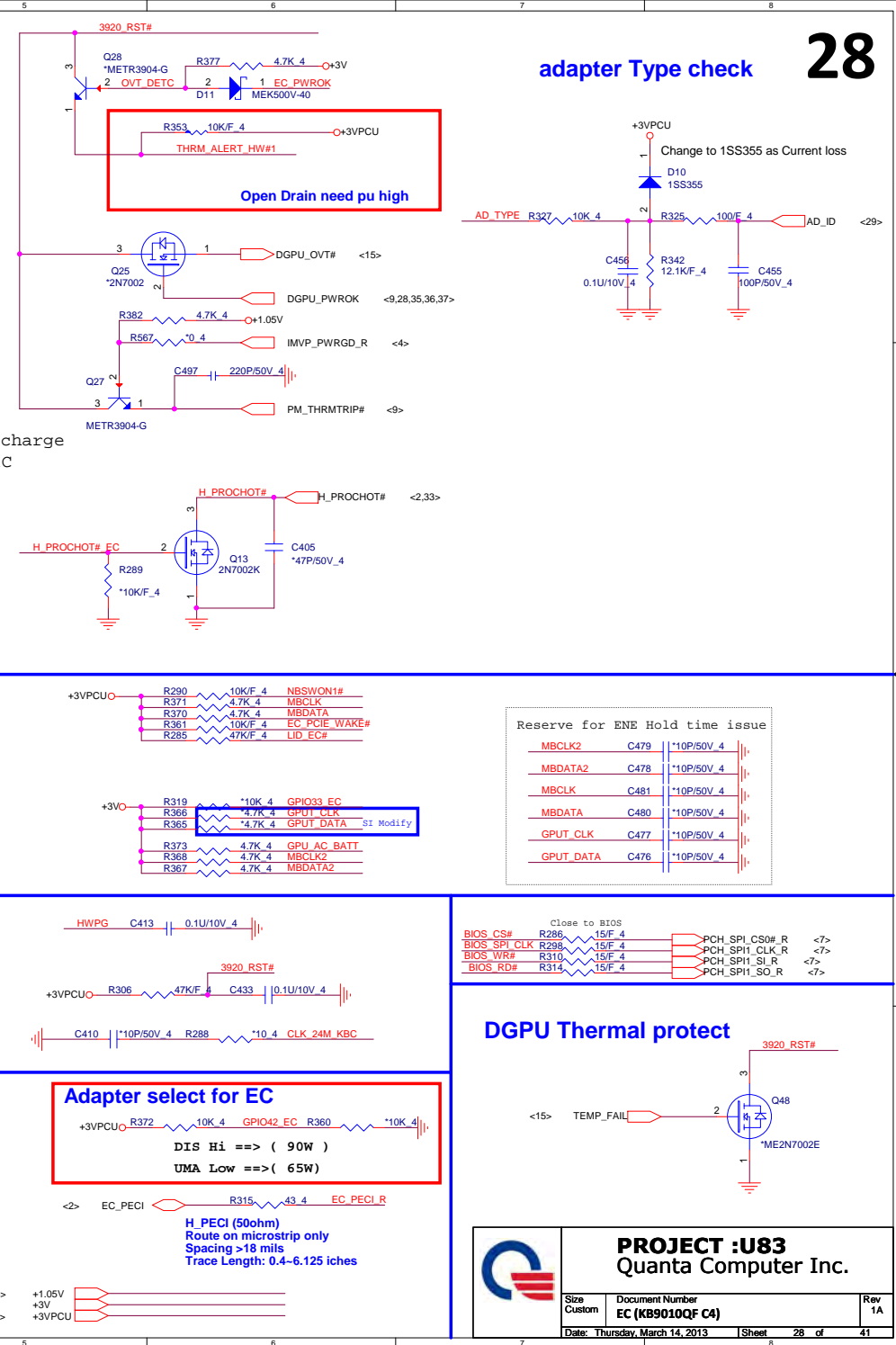
Touch screen

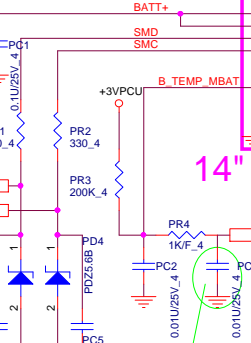


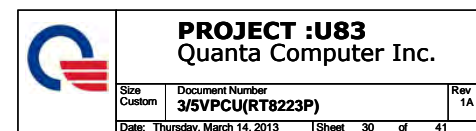
Green CLK Circuitry

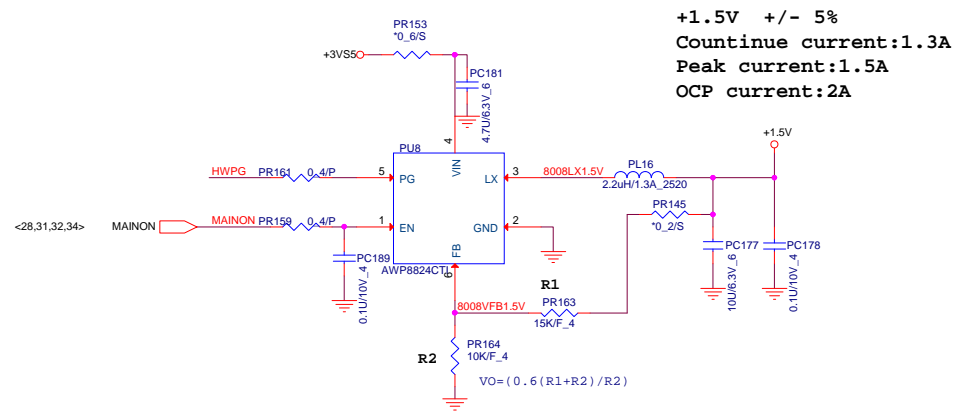
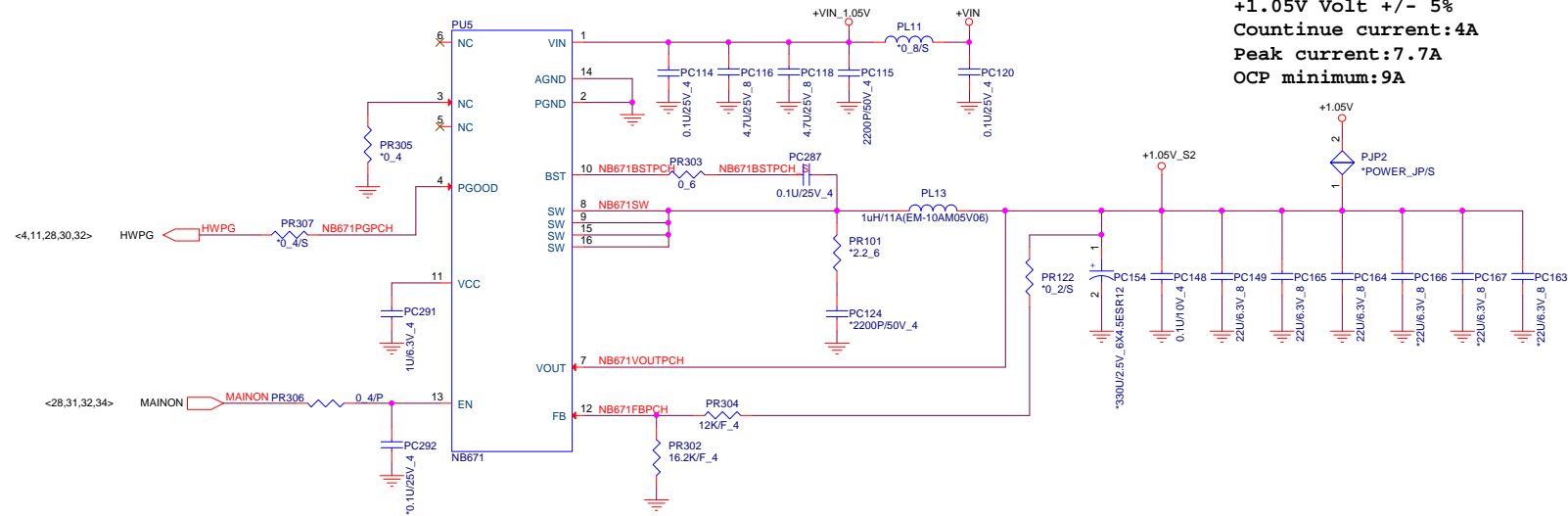


	P/N	R536	C434
UMA	AL003355000	N/A	N/A
DIS	AL003354001	Install	Install

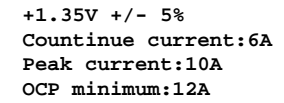


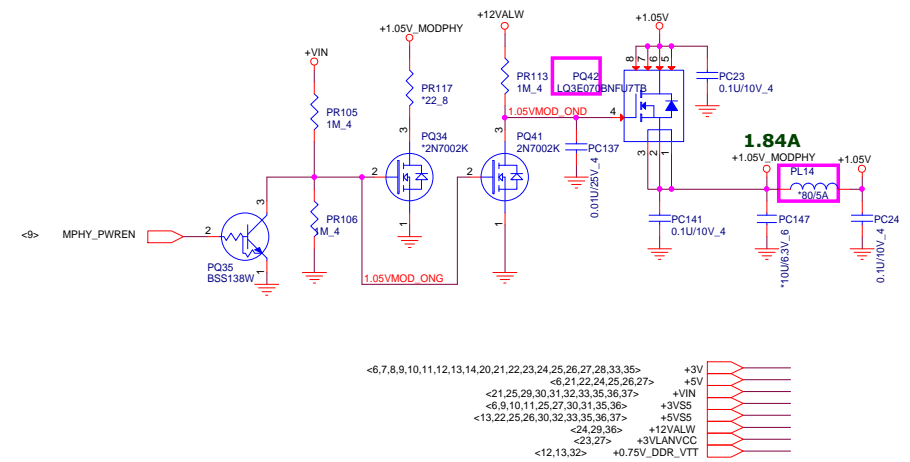


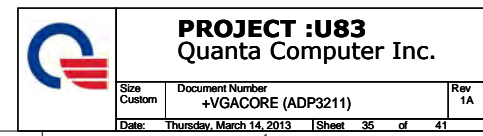
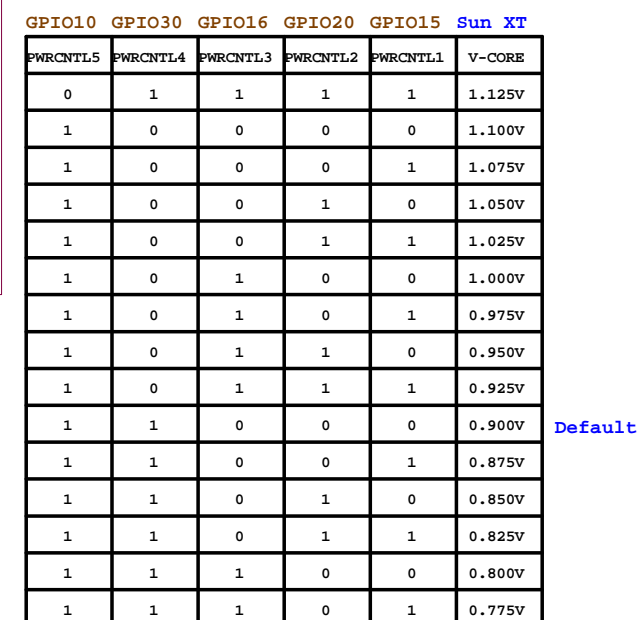


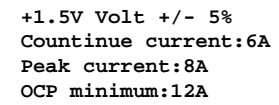


+VIN <21,25,29,30,32,33,34,35,36,37>
+3VSS <6,9,10,11,25,27,30,34,35,36>
+5VSS <13,22,25,26,30,32,33,34,35,36,37>
+5VPCU <13,29,30>









USB3.0	Port Assignment	Power control pin
PORT1	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT2	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT3	NC	N/A
PORT4	NC	N/A

USB2.0	Port Assignment	Power control pin
PORT0	USB2.0/USB3.0 COMBO 1st	USBPW_ON#(from EC)
PORT1	USB2.0/USB3.0 COMBO 2nd	USBPW_ON#(from EC)
PORT2	Camera	N/A
PORT3	NC	N/A
PORT4	NC	N/A
PORT5	Left side USB daughter B	USBPW_ON#(from EC)
PORT6	WLAN	N/A
PORT7	Touch Screen 15" used	TS_ON(from EC)

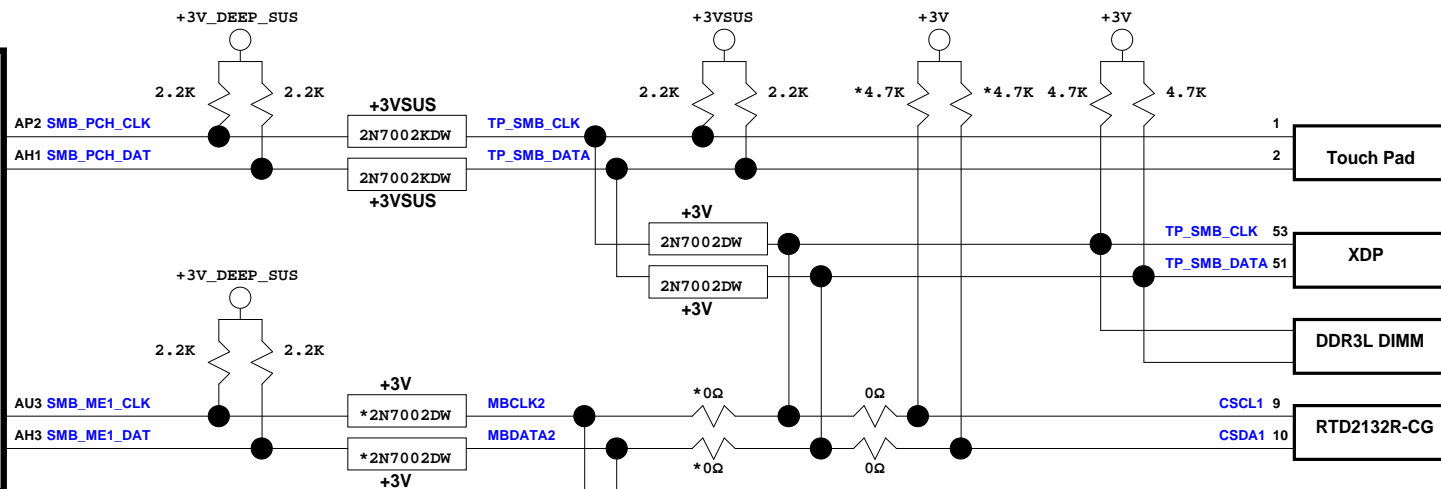
SATA Master	Port Assignment	Power control pin
SATA0	HDD	N/A
SATA1	mSATA	N/A
SATA2	NC	N/A
SATA3/PCIE	Card reader	N/A

PCIE	Port Assignment	Control pin
PCIE 5_L0	PEG0	
PCIE 5_L1	PEG1	
PCIE 5_L2	PEG2	
PCIE 5_L3	PEG3	
PCIE 1	NC	
PCIE 2	NC	
PCIE 3	WLAN	
PCIE 4	LAN	



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Haswell ULT



EC KB9010QF

